HT Series™
MTX Series™
PRO Series™

Professional Series
Two-Way Portable Radios

Detailed Service Manual

MOTOROLA

Document History

The following major changes have been implemented in this manual since the previous edition:

Edition	Description	Date
6881088E46-E	The Theory of Operation section has been divided into the following six sections: Distribution Keypad UHF Band 1 UHF Band 2 VHF Lowband, 800 MHz, PassPort, and 900 MHz	July, 2005
	Troubleshooting Flow Charts in the Maintenance section have updated.	
	Added 8480587Z05 to UHF Band 1	
	Added 8480450Z14 to UHF Band 1	
	Added 8486458Z02 to UHF Band 1	
	Added 8486458Z03 to UHF Band 1	
	Added 8415234H01 to UHF Band 1	
	Added 8485677Z03 to UHF Band 2	
	Added 8486686Z01 to UHF Band 2	
	Added 8486686Z02 to UHF Band 2	
	Added 8415235H01 to UHF Band 2	
	Added 8486062B16 to VHF	
	Added 8486062B17 to VHF	
	Added 8486101B11 to VHF	
	Added 8486473Z03 to VHF	
	Added 8486473Z04 to VHF	
	Added 8415112H01 to VHF	

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MTX Series™
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Professional Series
Two-Way Portable Radio

Detailed Service Manual

Motorola, Inc.
8000 West Sunrise Boulevard
Fort Lauderdale, Florida 33322

6881088C46-F

Foreword

The information contained in this manual relates to all models of the Professional Series two-way portable radios, unless otherwise specified. This manual provides sufficient information to enable qualified service shop technicians to troubleshoot and repair portable radios to the component level.

For details on the level 1 or 2 maintenance procedures, refer to the applicable manuals, which are available separately. A list of publications is provided in this manual in the section, "1.3 Related Documents" on page 1-2.

Product Safety and RF Exposure Compliance

Before using this product, read the operating instructions for safe usage contained in the Product Safety and RF Exposure booklet enclosed with your radio.

ATTENTION!

This radio is restricted to occupational use only to satisfy FCC RF energy exposure requirements. Before using this product, read the RF energy awareness information and operating instructions in the Product Safety and RF Exposure booklet enclosed with your radio (Motorola Publication part number 6881095C98) to ensure compliance with RF energy exposure limits.

For a list of Motorola-approved antennas, batteries, and other accessories, visit the following web site which lists approved accessories: http://www.motorola.com/cgiss/index.shtml

Manual Revisions

Changes which occur after this manual is printed are described in FMRs (Florida Manual Revisions). These FMRs provide complete replacement pages for all added, changed, and deleted items, including pertinent parts list data, schematics, and component layout diagrams.

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Trademarks

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Intrinsically Safe Radio Information

FMRC Approved Equipment

Anyone intending to use a radio in a location where hazardous concentrations of flammable materials exist (hazardous atmosphere) is advised to become familiar with the subject of intrinsic safety and with the National Electric Code NFPA 70 (National Fire Protection Association) Article 500 (hazardous [classified] locations).

An Approval Guide, issued by Factory Mutual Research Corporation (FMRC), lists manufacturers and the products approved by FMRC for use in such locations. FMRC has also issued a voluntary approval standard for repair service (“Class Number 3605”).

FMRC Approval labels are attached to the radio to identify the unit as being FM Approved for specified hazardous atmospheres. This label specifies the hazardous Class/Division/Group along with the part number of the battery that must be used. Depending on the design of the portable unit, this FM label can be found on the back or the bottom of the radio housing. The FM Approval mark is shown below.

- **Do not operate radio communications equipment in a hazardous atmosphere unless it is a type especially qualified (for example, FMRC Approved) for such use. An explosion or fire may result.**
- **Do not operate an FMRC Approved Product in a hazardous atmosphere if it has been physically damaged (for example, cracked housing). An explosion or fire may result.**
- **Do not replace or charge batteries in a hazardous atmosphere. Contact sparking may occur while installing or removing batteries and cause an explosion or fire.**
- **Do not replace or change accessories in a hazardous atmosphere. Contact sparking may occur while installing or removing accessories and cause an explosion or fire.**
- **Turn a radio off before removing or installing a battery or accessory.**
- **Do not disassemble an FMRC Approved Product unit in any way that exposes the internal electrical circuits of the unit.**

Radios must ship from the Motorola manufacturing facility with the Intrinsically Safe, hazardous atmosphere capability and FM Approval labeling. Radios will not be “upgraded” or converted to Intrinsically safe, and or labeled in the field, after it has been shipped from the manufacturing location.

Modifications can only be made by the original product manufacturer (Motorola) at one of its FM audited manufacturing facilities.

- **Failure to use an FMRC Approved portable radio unit with an FMRC Approved battery or FMRC Approved accessories specifically Agency approved for that product may result in the dangerously unsafe condition of an unapproved radio combination being used in a hazardous location.**
- **Unauthorized or incorrect modification of an FMRC Approved Product unit will negate the Approval rating of the product.**

Repair of FMRC Approved Products

REPAIRS FOR MOTOROLA PRODUCTS WITH FMRC APPROVAL ARE THE RESPONSIBILITY OF THE USER.

You should not repair or relabel any Motorola- manufactured communication equipment bearing the FMRC Approval label (“FMRC Approved Product”) unless you are familiar with the current FMRC Approval standard for repairs and service (“Class Number 3605”). Repairs and service to be done FM audited locations.

- **Incorrect repair or relabeling of any FMRC Approved Product unit could adversely affect the Approval rating of the unit.**
- **Use of a radio that is not intrinsically safe in a hazardous atmosphere could result in serious injury or death.**

The following are key definitions, from the FMRC’s Approval Standard Class Number 3605, 1994.

Repair

A repair constitutes something done internally to the unit that would bring it back to its original condition-Approved by FMRC. A repair should be done in an FMRC audited facility. Items not considered as repairs are those in which an action is performed on a unit which does not require the outer casing of the unit to be opened in a manner which exposes the internal electrical. You do not have to be an FMRC audited Repair Facility to perform these actions.

Relabeling

The repair facility shall have a method by which the replacement of FMRC Approval labels are controlled to ensure that any relabeling is limited to units that were originally shipped from the Manufacturer with an FM Approval label in place. FMRC Approval labels shall not be stocked by the repair facility. An FMRC Approval label shall be ordered from the original manufacturer, as needed, to repair a specific unit. Replacement labels may be obtained and applied by the repair facility, provided there is satisfactory evidence that the unit being relabeled was originally an FMRC Approved unit. Verification may include, but is not limited to: a unit with a damaged Approval label, a unit with a defective housing displaying an Approval label, or a customer invoice indicating the serial number of the unit and purchase of an FMRC Approved model.

Do Not Substitute Options or Accessories

The Motorola communications equipment certified by Factory Mutual is tested as a system and consists of the FM Approved portable, FM Approved battery, and FM Approved accessories or options, or both. This FM Approved portable and battery combination must be strictly observed. There must be no substitution of items, even if the substitute has been previously Approved with a different Motorola communications equipment unit. Approved configurations are listed in the FM Approval Guide published by FMRC, or in the product FM product listing. This FM product listing is shipped from the manufacturer with the FM Approved radio and battery combination.

Notes

Chapter 1 Introduction

1.1 Scope of Manual

This manual is intended for use by service technicians familiar with similar types of equipment. It contains service information required for the equipment described and is current as of the printing date. Changes that occur after the printing date are incorporated by a complete manual revision or alternatively, as additions.

NOTE: Before operating or testing these units, please read the sections, "Product Safety and RF Exposure Compliance" on page ii and "Intrinsically Safe Radio Information" on page xix.

1.2 Warranty and Service Support

Motorola offers long term support for its products. This support includes full exchange and/or repair of the product during the warranty period, and service/repair or spare parts support out of warranty. Any “return for exchange” or “return for repair” by an authorized Motorola dealer must be accompanied by a warranty claim form. Warranty claim forms are obtained by contacting customer service.

1.2.1 Warranty Period

The terms and conditions of warranty are defined fully in the Motorola dealer or distributor or reseller contract. These conditions may change from time to time and the following notes are for guidance purposes only.

1.2.2 Return Instructions

In instances where the product is covered under a “return for replacement” or “return for repair” warranty, a check of the product should be performed prior to shipping the unit back to Motorola. This is to ensure that the product has been correctly programmed or has not been subjected to damage outside the terms of the warranty.

Prior to shipping any radio back to a Motorola warranty depot, please contact the appropriate customer service for instructions. All returns must be accompanied by a warranty claim form, available from your customer services representative. Products should be shipped back in the original packaging, or correctly packaged to ensure no damage occurs in transit.

1.2.3 After Warranty Period

After the Warranty period, Motorola continues to support its products in two ways:

First, Motorola's Customer Care and Services Division offers a repair service to both end users and dealers at competitive prices.

Second, Motorola’s service department supplies individual parts and modules that can be purchased by dealers who are technically capable of performing fault analysis and repair.

1.3 Related Documents

The following documents are directly related to the use and maintainability of this product.

Table 1-1. Related Documents

Title	Part Number
Professional Radio Portable Level 1&2 Basic Service Manual- English (North America)	68P80906Z54
Professional Radio Portable Level 1&2 Basic Service Manual- English (Latin America)	68P81088C45
Professional Radio Portable Level 1&2 Basic Service Manual- Spanish	68P81088C47
Professional Radio Portable Level 1&2 Basic Service Manual- Portuguese	68P81088C49
Professional Radio Portable Service Manual Level 3 - English	68P81088C46
Professional Radio Portable Service Manual Level 3 - Spanish	68P81088C48
Professional Radio Portable Service Manual Level 3 - Portuguese	68P81088C50
Supplement to Professional Radio Portable Level 1&2 Basic Service Manual	68P81093C57

1.4 Technical Support

Technical support is available to assist the dealer/distributor and self-maintained customers in resolving any malfunction which may be encountered. Initial contact should be by telephone to customer resources wherever possible. When contacting Motorola technical support, be prepared to provide the product model number and the unit's serial number. The contact locations and telephone numbers are located in the applicable basic service manual listed in Table 1-1 above.

1.4.1 Piece Parts Availability

Some replacement parts, spare parts, and/or product information can be ordered directly. If a complete Motorola part number is assigned to the part, and it is not identified as "Depot ONLY", the part is available from Motorola Customer Care and Services Division. If no part number is assigned, the part is not normally available from Motorola. If the part number is appended with an asterisk, the part is serviceable by a Motorola depot only. If a parts list is not included, this generally means that no user-serviceable parts are available for that kit or assembly.

Parts Order Entry
7:00 A.M. to 7:00 P.M. (Central Standard Time)
Monday through Friday (Chicago, U.S.A.)

To Order Parts in the United States of America:
1-800-422-4210, or 847-538-8023
1-800-826-1913, or 410-712-6200 (U.S. Federal Government)
TELEX: 280127
FAX: 1-847-538-8198
FAX: 1-410-712-4991 (U.S. Federal Government)
(U.S.A.) after hours or weekends:
1-800-925-4357

To Order Parts in Latin America and the Caribbean:
1-847-538-8023

Motorola Parts
(United States and Canada)
Customer Care and Services Division
Attention: Order Processing
1307 E. Algonquian Road
Schaumburg, IL 60196

Customer Care and Services Division
Attention: Latin America and Caribbean

Order Processing
1307 E. Algonquian Road
Schaumburg, IL 60196

Parts Identification
1-800-422-4210, menu 3

1.5 Radio Model Chart and Specifications

The radio model charts and specifications are located in the Basic Service Manual listed under the Related Documents paragraph of this chapter.

1.6 Radio Model Information

The model number and serial number are located on a label attached to the back of your radio. You can determine the RF output power, frequency band, protocols, and physical packages from these numbers. The example in Table 1-2 on page 1-4 shows one portable radio model number and its specific characteristics.

.

Table 1-2. Radio Model Number

Example: AAH25KC9AA2 and LAH25KDC9AA3

	Type of Unit	Model Series	Freq. Band	Power Level	Physical Packages	Channel Spacing	Protocol	Feature Level	Model Revision	Model Package
AA or **LA** ↑ **AA or LA** = Motorola Internal Use →	**H** ↑ **H** = Portable →	**25**	**K** VHF (136-174 MHz)	**C** 2.5W	**C** No Display	**9** Program-mable	**AA** Conven-tional	**2** 2F for AA 4F for LA	**A**	**N**
			R UHF1 (403-470 MHz)	**D** 4-5W	**D** Keypad	**6** 25 kHz	**DU** LTR	**3** 16F		
			S UHF2 (450-527 MHz)	**E** 6W	**H** 1-Line Display		**CK** MPT	**5** 256F LTR for AA only		
			B Low Band, R1 (29.7-42.0 MHz)				**GB** Privacy Plus	**6** 128F 256F LTR		
			C Low Band, R2 (35.0-50.0 MHz)				**GE** Privacy Plus Roaming	**8** 160F		
			U 800 MHz (806-824) (851-869 MHz)				**DP** PassPort and LTR	**7** 256F LTR		
							FC Smart Zone	**9** 256F LTR		

Chapter 2 Radio Power Distribution

A block diagram of the DC power distribution throughout the radio board is shown in Figure 2-1. A 7.5V battery supplies the basic radio power (UNSWB) directly to the electronic on/off control, audio power amplifier, 3.5V regulator, power amplifier automatic level control (ALC), and low battery detect circuit. When the radio on/off/volume control is turned on, the switched SWB+ is applied to the various radio power regulators, antenna switch, accessories 20-pin connector, keypad/option board, and transmit LED. The Vdda signal from the 3.3V Vdda regulator supplies the microprocessor with operating power. The Vdd regulator scheme is listed by band in Table 2-1 on page 2-1. Data is then sent to the controller ASFIC to turn on a DAC which takes over the momentary-on path within 12ms. The SWB+ signal supplies power until the radio is turned off. Jumpers for configuring the Vdda and Vddd regulators are shown in Figure 2-1 and described in Table 2-2 on page 2-2.

The radio turns off when either of the two following conditions occur:

- Radio on/off/volume control is turned off.
- Low battery condition is detected.

If a low battery level is detected by the microprocessor through either of the above conditions, the radio personality data is stored to EEPROM prior to turning off.

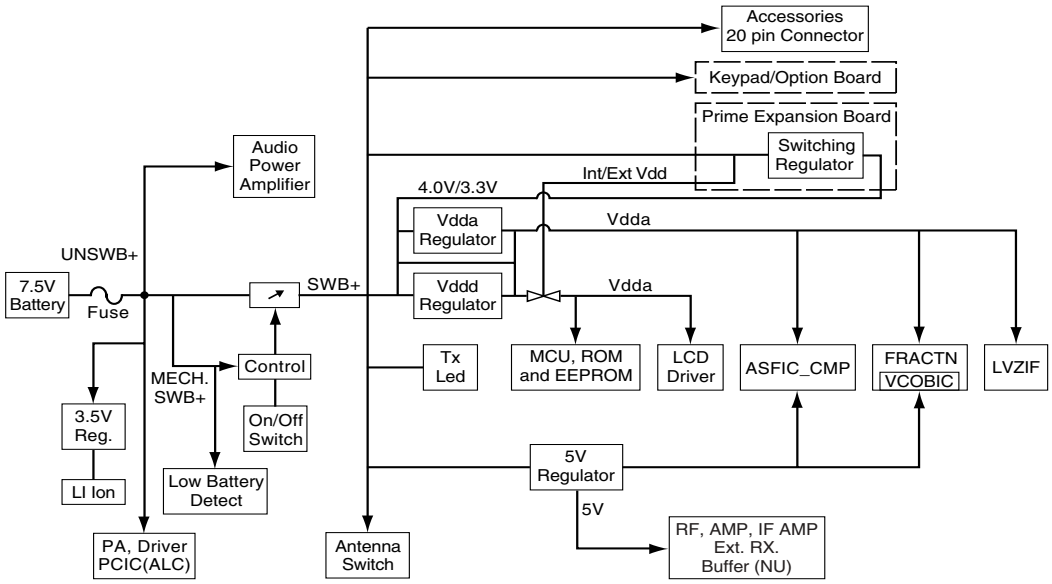

Figure 2-1. DC Power Distribution Block Diagram

Table 2-1. VDD Regulator Scheme by Band

Band	Vdd Regulator Scheme
Low Band	Dual

Table 2-1. VDD Regulator Scheme by Band

Band	Vdd Regulator Scheme
VHF	Dual
UHF	Dual
800 MHz	Dual
900 MHz	Dual

Table 2-2. Radio Jumpers

Jumpers	Dual Vdd Regulator Scheme	Single Vdd Regulator Scheme
R401	Y	Y
R402	N	N
R403	N	Y
R404	N	N
R405	Y	N

R = Regulator Jumper

Chapter 3 Keypad

The keypad block diagram is shown in Figure 3-1. The comparator compares the voltage when any one of the keypad row or keypad column keys is pressed. Pressing a key sends a message to the microprocessor through the output (KEY_INT) line signifying that a key has been pressed. The microprocessor then samples the analog to digital voltages at the keypad row and keypad column, then makes a comparison with a map table to identify the key pressed. Once the key is identified, a corresponding message is displayed.

The LED_EN is set by the codeplug. When the value is set to low, the LED lights up during power up. A high codeplug setting disables this feature.

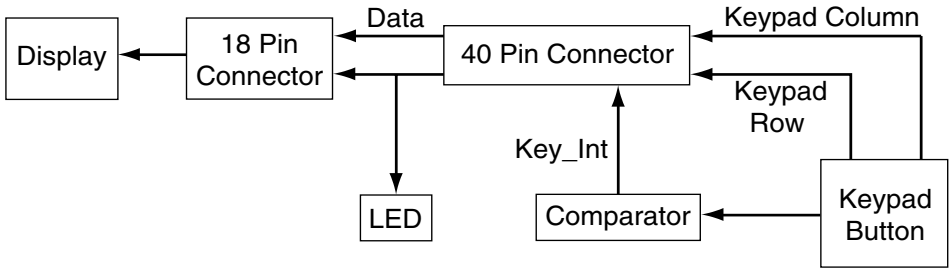

Figure 3-1. Keypad Block Diagram

3.1 Controller Board

The controller board is the central interface between the various radio functions. It is separated into MCU digital and audio/signalling functions as shown in Figure 3-2.

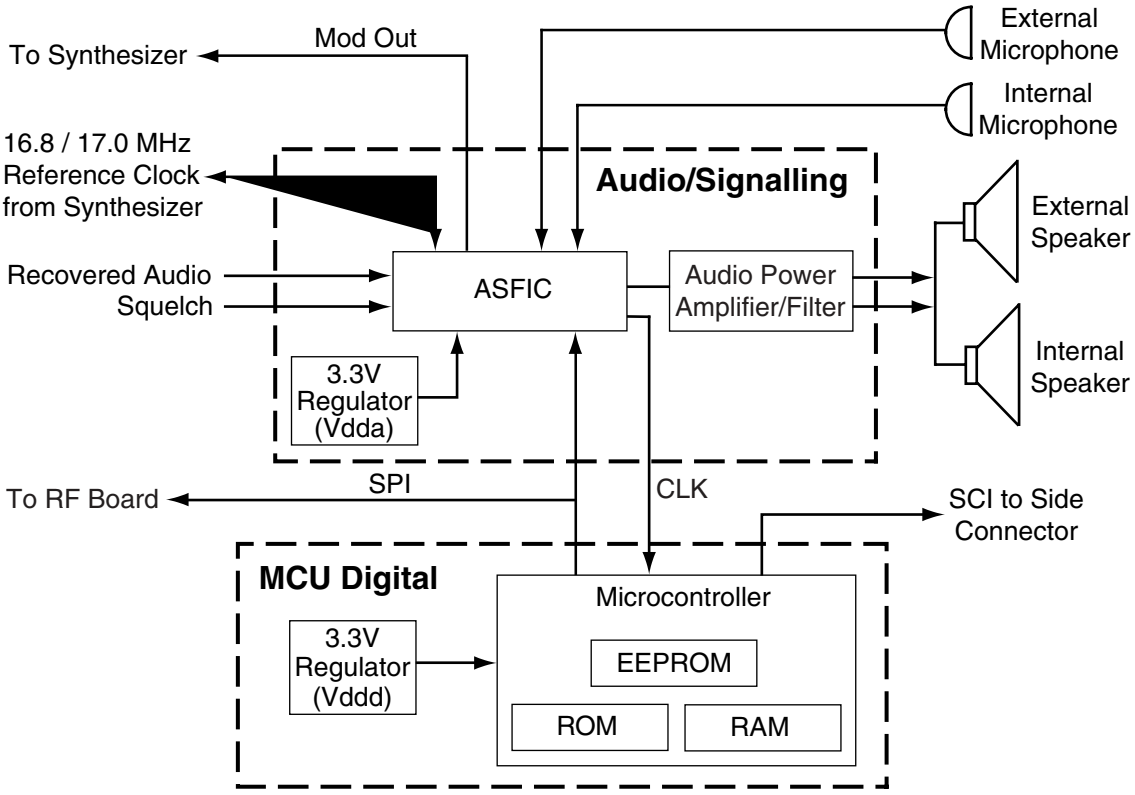

Figure 3-2. Controller Block Diagram

3.1.1 MCU Digital

The digital portion of the controller consists of a microcontroller and associated EEPROM, RAM, and ROM memories. Combinations of different size RAM and ROM are available to support various application software. RAM supports 8KB and 32KB sizes. ROM supports 128KB, 256KB, and 512KB sizes. Table 3-1 lists the ROM, RAM and EEPROM requirements for different radios.

Table 3-1. Radio Memory Requirements

PROTOCOL	FEATURE LEVEL	ROM (KB)	EXT RAM (KB)	EEPROM (KB)
AA,DU	2 or 3	128	-	8
AA,DU	6	128	-	16
CK, GB, GE, FC	-	512	32	16

3.1.2 Real Time Clock

Radios with displays support a real time clock (RTC) module for purposes of message time stamping and time keeping. The RTC module resides in the microcontroller. The clock uses a back-up lithium-ion battery for operating power when the primary battery is removed.

3.1.3 Circuit Description

The RTC module circuit, shown in Figure 3-3, is powered by the MODB/VSTBY pin and PI6/PI7 from the crystal oscillator circuit. A clock frequency of 38.4 kHz from a crystal oscillator provides the reference signal which is divided down to 1 Hz in the processor.

As the RTC module is powered separately from the processor Vdd, the RTC is kept active through the MODB/VSTBY pin which provides the lithium-ion battery back-up power when the radio is switched off.

A MOSFET transistor (Q416) switches in the battery supply when Vdd is removed. Q416 also provides isolation from BOOT_CTRL function. The 3.3 V regulator charges the lithium-ion battery.

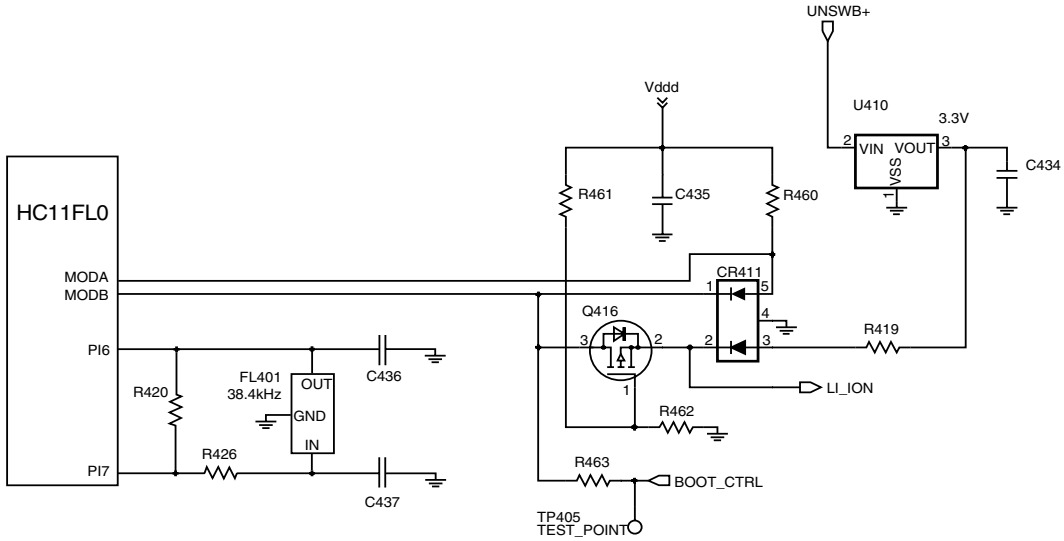

Figure 3-3. RTC Circuit

3.1.4 MODB/VSTBY Supply

The supply to the MODB/VSTBY pin varies depending on the conditions listed in Table 3-2.

Table 3-2. MODB/VSTBY Supply Modes

Condition	Circuit Operation
Radio On	Vddd supply voltage via CR411
Radio Off	• Vddd turned off • Q416 gate pulled low by R462 • Q416 switched on • U410 supplies 3.2V to MODB_VSTBY
Primary battery removed	• Vddd turned off • Q416 gate pulled low by R462 • Q416 switched on • Lithium-ion battery provides 3.2V to MODB_VSTBY

3.1.5 Audio/Signaling

The audio/signalling/filter/companding IC (ASFIC) and the audio power amplifier (Figure 3-2 on page 3-2) form the main components of the audio/signalling section of the controller board. Inputs include a 16.8 MHz clock from the synthesizer, recovered audio and squelch, MCU control signals, and external or internal microphones. Outputs include a microprocessor clock (CLK), modulator output to the synthesizer, and amplified audio signals to an internal or external speaker.

Chapter 4 UHF Band 1 Theory of Operation

4.1 Transmitter

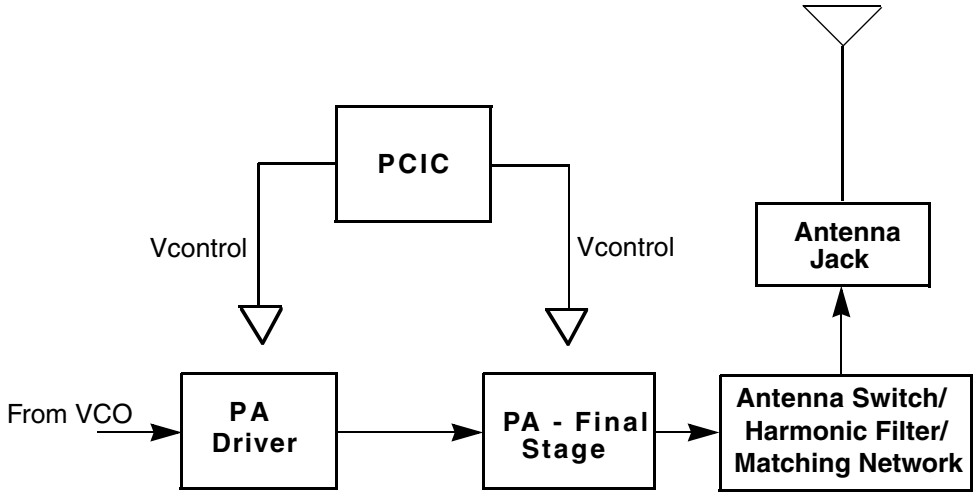

Figure 4-1. Transmitter Block Diagram

4.1.1 General

(Refer to Figure 4-1.)

The UHF transmitter contains five basic circuits:

- Power amplifier
- Antenna switch
- Harmonic filter
- Antenna matching network
- Power control integrated circuit (PCIC)

4.1.2 Power Amplifier

The power amplifier consists of two devices:

- 9Z67 LDMOS driver IC (U101)
- PRF1507 LDMOS PA (Q110)

The 9Z67 LDMOS driver IC contains a two-stage amplification with a supply voltage of 7.3 V.

This RF power amplifier is capable of supplying an output power of 0.3 W (pin 6 and 7) with an input signal of 2 mW (3 dBm) (pin16). The current drain would typically be 160mA while operating in the frequency range of 403-470MHz.

The PRF1507 LDMOS PA is capable of supplying an output power of 7 W with an input signal of 0.3 W. The current drain would typically be 1300mA while operating in the frequency range of 403-470 MHz. The power output can be varied by changing the biasing voltage.

4.1.3 Antenna Switch

The antenna switch circuit consists of two PIN diodes (CR101 and CR102), a pi network (C107, L104 and C106), and two current limiting resistors (R101, R170). In the transmit mode, B+ at PCIC (U102) pin 23 will go low and turn on Q111 where a B+ bias is applied to the antenna switch circuit to bias the diodes “on”. The shunt diode (CR102) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

4.1.4 Harmonic Filter

The harmonic filter consists of C104, L102, C103, L101 and C102. The design of the harmonic filter for UHF is that of a modified Zolotarev design. It has been optimized for efficiency of the power module. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically less than 1.2dB.

4.1.5 Antenna Matching Network

A matching network which is made up of L116 is used to match the antenna's impedance to the harmonic filter. This will optimize the performance of the transmitter and receiver into an antenna.

4.1.6 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U102 to regulate the power output of the radio. The current to the final stage of the power module is supplied through R101, which provides a voltage proportional to the current drain. This voltage is then fed back to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C133, C134 and C135) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

CR105 and its associated components are part of the temperature cut-back circuitry. It senses the printed circuit board temperature around the transmitter circuits and output a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

4.2 Receiver

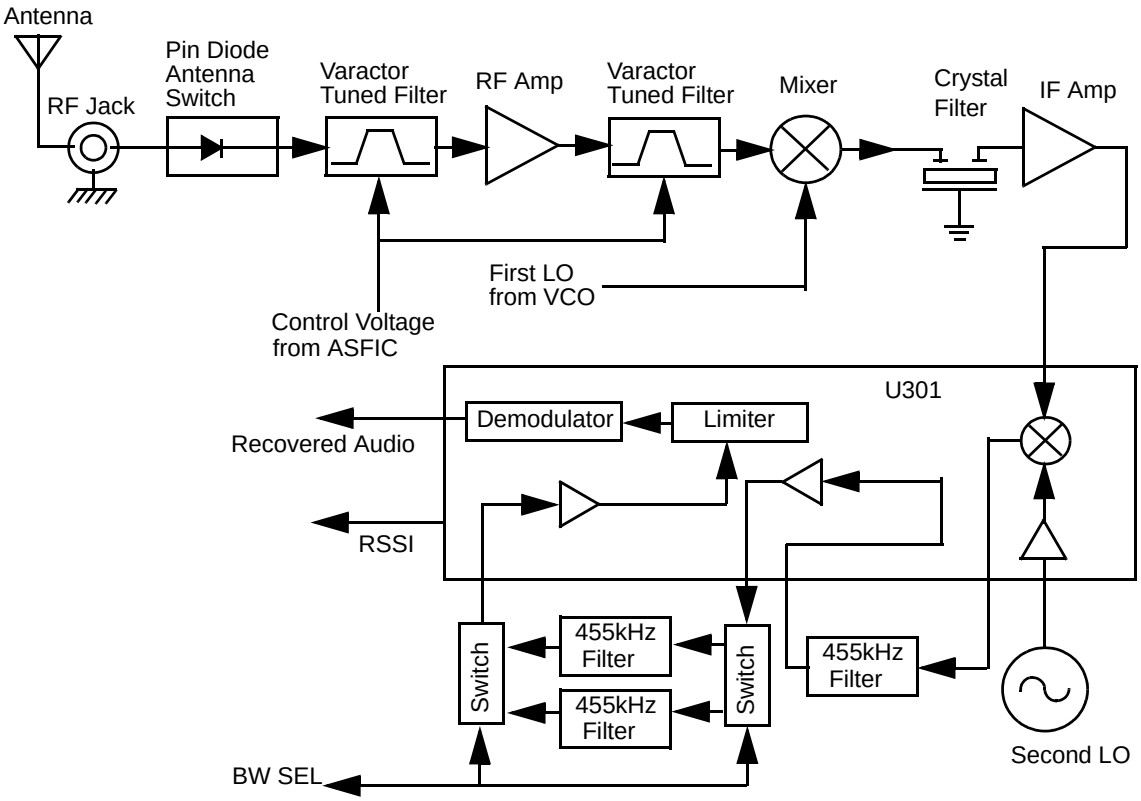

Figure 4-2. UHF Receiver Block Diagram

4.2.1 Receiver Front-End

(Refer to the *UHF Receiver Front-End Schematic Diagram* on page 9-84 and the *UHF Transmitter Schematic Diagram* on page 9-89.)

The RF signal is received by the antenna and applied to a low-pass filter. For UHF, the filter consists of L101, L102, C102, C103, C104. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes (CR101 and CR102) and a pi network (C106, L104 and C107).The signal is then applied to a varactor tuned bandpass filter. The UHF bandpass filter comprises of L301, L302, C302, C303, C304, CR301 and CR302. The bandpass filter is tuned by applying a control voltage to the varactor diodes (CR301 and CR302) in the filter.

The bandpass filter is electronically tuned by the DACRx from IC404 which is controlled by the microprocessor. Depending on the carrier frequency, the DACRx will supply the tuned voltage to the varactor diodes in the filter. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q301 via C307. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L306, L307, C313, C317, CR304 and CR305.

Both the pre and post-RF amplifier varactor tuned filters have similar responses. The 3 dB bandwidth of the filter is about 50 MHz. This enables the filters to be electronically controlled by using a single control voltage which is DACRx.

The output of the post-RF amplifier filter which is connected to the passive double balanced mixer consists of T301, T302 and CR306. Matching of the filter to the mixer is provided by C381. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to the 44.85 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL301) through a resistor pad and a diplexer (C322 and L310). Matching to the input of the crystal filter is provided by C324 and L311. The crystal filter provides the necessary selectivity and intermodulation protection.

4.2.2 Receiver Back-End

(Refer to *UHF Receiver Back-End Schematic Diagram* on page 9-85.)

The output of crystal filter FL301 is matched to the input of first IF amplifier transistor Q302 by L330. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The IF amplifier provides a gain of about 16dB. The amplified first IF signal is then coupled into U301 (pin 1) via C360 and L332 which provides the matching for the first IF amplifier and U301.

Within U301, the first IF 44.85 MHz signal mixes with the 44.395 MHz second local oscillator (2nd LO) to produce the second IF signal at 455 kHz. The second LO signal frequency is determined by crystal Y300. The second IF signal (455 kHz) is then filtered by an external ceramic filter FL302 before being amplified by the second IF amplifier within U301. Again, the signal is filtered by a second external ceramic filter FL303 or FL304 depending on the selected channel spacing. FL303 is used for 20/25 kHz channel spacing whereas FL304, for 12.5 kHz channel spacing. The simple circuit consisting of U302, CR312, CR313 and resistors R345, R360, R321 and R324 divert the second IF signal according to the BW_SEL line. The filtered output of the second IF signal is applied to the limiter input pin of U301.

The IF IC (U301) contains a quadrature detector using a ceramic phase-shift element (Y301) to provide audio detection. Internal amplification provides an audio output level around 120mVrms (@60% deviation) from pin 8 of U301. This demodulated audio is fed to the ASFIC_CMP IC (U404) in the controller section.

The IF IC (U301) also performs several other functions. It provides a received signal-strength indicator (RSSI) with a dynamic range of 70 dB. The RSSI is a dc voltage monitored by the microprocessor, and used as a peak indicator during the bench tuning of the receiver front-end varactor filter.

4.3 Frequency Generation Circuitry

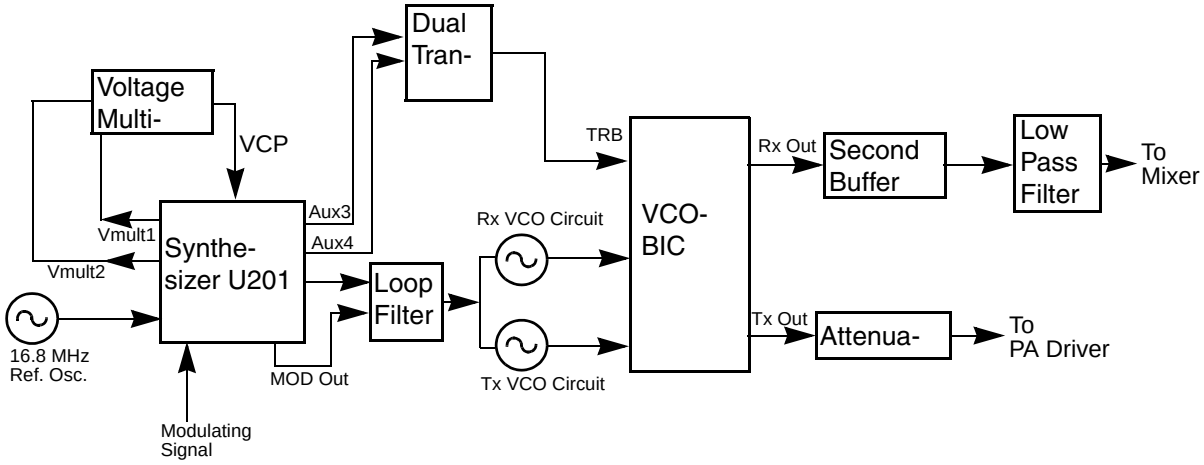

Figure 4-3. Frequency Generation Unit Block Diagram

The Frequency Generation Circuitry is composed of two main ICs:

- Fractional-N synthesizer (U201)
- VCO/Buffer IC (U241)

Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5 V and 3.3 V which come from U247 and U248 respectively. The synthesizer in turn generates a super-filtered 4.5 V which powers U241.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3 V dc signal from the synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin 10 of U201. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

4.4 Synthesizer

(Refer to *UHF Synthesizer Schematic Diagram* on page 9-86.)

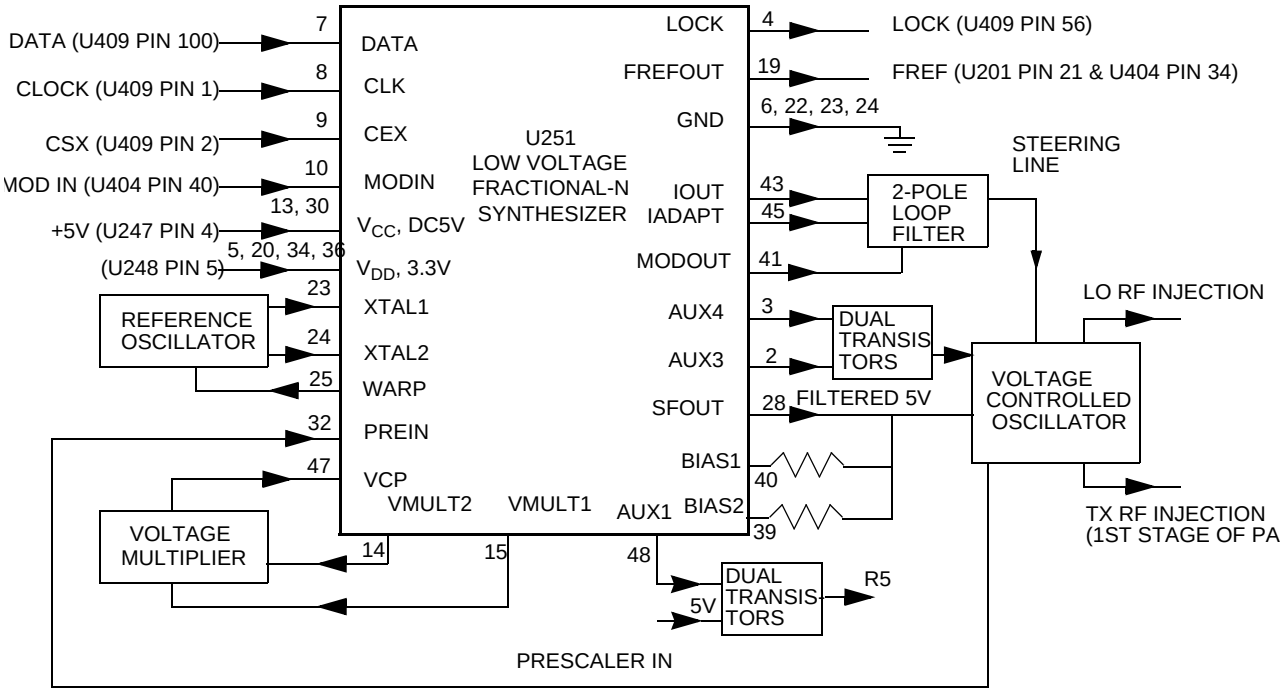

Figure 4-4. Synthesizer Block Diagram

The Fractional-N Synthesizer uses a 16.8MHz crystal (FL201) to provide a reference for the system. The LVFractN IC (U201) further divides this to 2.1 MHz, 2.225 MHz, and 2.4 MHz as reference frequencies. Together with C206, C207, C208, R204 and CR203, they build up the reference oscillator which is capable of 2.5ppm stability over temperatures of -30 to 85°C. It also provides 16.8 MHz at pin 19 of U201 to be used by the ASFIC.

The loop filter which consist of C231, C232, C233, R231, R232 and R233 provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put synthesizer within the lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier which is made up of C258, C259, C228, triple diode CR201 and level shifters U210 and U211. Two 3.3V square waves (180 degrees out of phase) are first shifted to 5V, then along with regulated 5V, put through arrays of diodes and capacitors to build up 13.3V at pin 47 of U201.

4.5 Voltage-Controlled Oscillator (VCO)

(Refer to the *UHF Voltage-Controlled Oscillator Schematic Diagram* on page 9-87.)

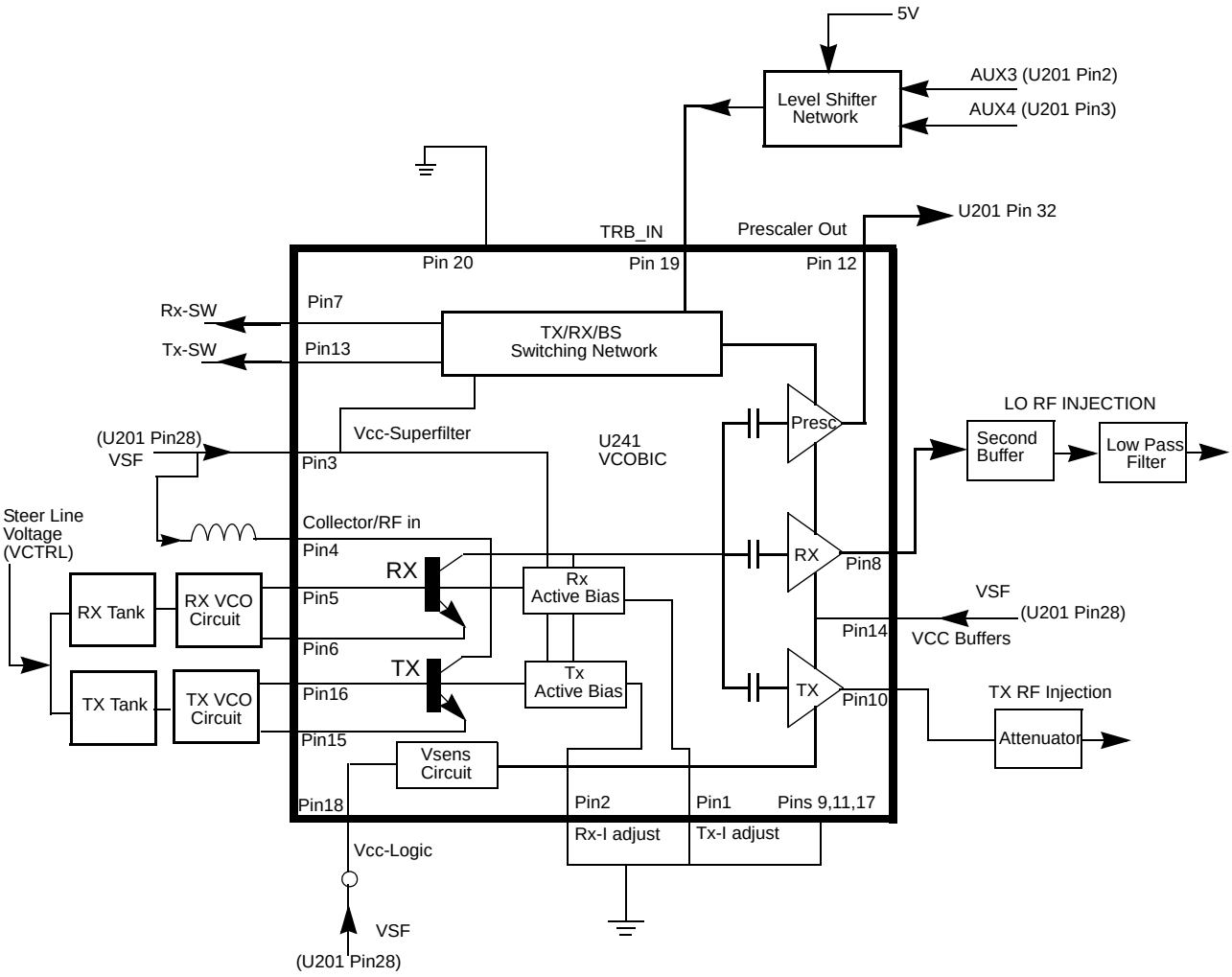

Figure 4-5. VCO Block Diagram

The VCOBIC (U241) in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U241 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U241 pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a dc voltage between 3.5 V and 9.5 V when the PLL is locked on frequency.

The VCOBIC (U241) is operated at 4.54 V (VSF) and Fractional-N synthesizer (U201) at 3.3 V. This difference in operating voltage requires a level shifter consisting of Q260 and Q261 on the TRB line.

The operation logic is shown in Table 4-1.

Table 4-1. Level Shifter Logic

Desired Mode	AUX 4	AUX 3	TRB
Tx	Low	High (@3.2V)	High (@4.8V)
Rx	High	Low	Low
Battery Saver	Low	Low	Hi-Z/Float (@2.5V)

In receive mode, U241 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U241. The RF signal at U241 pin 8 is run through a second buffer to improve mixer to receive VCO isolation. The resulting RF signal is LO RF INJECTION and it is applied to the mixer at T302. (Refer to the *UHF Receiver Front-End Schematic Diagram* on page 9-84.)

During the transmit condition, when PTT is depressed, a five-volt current is applied to U241 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U241. The RF signal at U241 pin 10 is injected into the input of the PA module (U101 pin16). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through the U201 pin 41.

When a high impedance is applied to U241 pin 19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

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Chapter 5 UHF Band 2 Theory of Operation

5.1 Transmitter

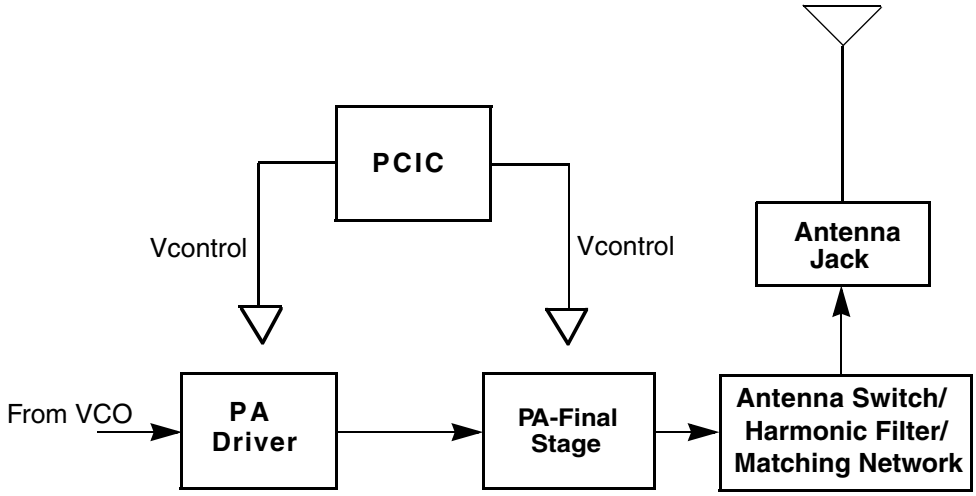

Figure 5-1. Transmitter Block Diagram

5.1.1 General

(Refer to Figure 5-1)

The UHF transmitter contains five basic circuits:

- power amplifier
- antenna switch
- harmonic filter
- antenna matching network
- power control integrated circuit (PCIC)

5.1.2 Power Amplifier

The power amplifier consists of two devices:

- 9Z67 LDMOS driver IC (U101)
- PRF1507 LDMOS PA (Q110)

The 9Z67 LDMOS driver IC contains a 2 stage amplification with a supply voltage of 7.3 V.

This RF power amplifier is capable of supplying an output power of 0.3 W (pin 6 and 7) with an input signal of 2 mW (3 dBm) (pin16). The current drain would typically be 160 mA while operating in the frequency range of 450-527 MHz.

The PRF1507 LDMOS PA is capable of supplying an output power of 7 W with an input signal of 0.3 W. The current drain would typically be 1300 mA while operating in the frequency range of 450-527 MHz. The power output can be varied by changing the biasing voltage.

5.1.3 Antenna Switch

The antenna switch circuit consists of two PIN diodes (CR101 and CR102), a pi network (C107, L104 and C106), and two current limiting resistors (R101, R170). In the transmit mode, B+ at PCIC (U102) pin 23 will go low and turn on Q111 where a B+ bias is applied to the antenna switch circuit to bias the diodes "on." The shunt diode (CR102) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

5.1.4 Harmonic Filter

The harmonic filter consists of C104, L102, C103, L101 and C102. The design of the harmonic filter for UHF is that of a modified Zolotarev design. It has been optimized for efficiency of the power module. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically less than 1.2 dB.

5.1.5 Antenna Matching Network

A matching network which is made up of L116 is used to match the antenna's impedance to the harmonic filter. This will optimize the performance of the transmitter and receiver into an antenna.

5.1.6 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U102 to regulate the power output of the radio. The current to the final stage of the power module is supplied through R101, which provides a voltage proportional to the current drain. This voltage is then fed back to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C133, C134 and C135) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

CR105 and its associated components are part of the temperature cut back circuitry. It senses the printed circuit board temperature around the transmitter circuits and output a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

5.2 Receiver

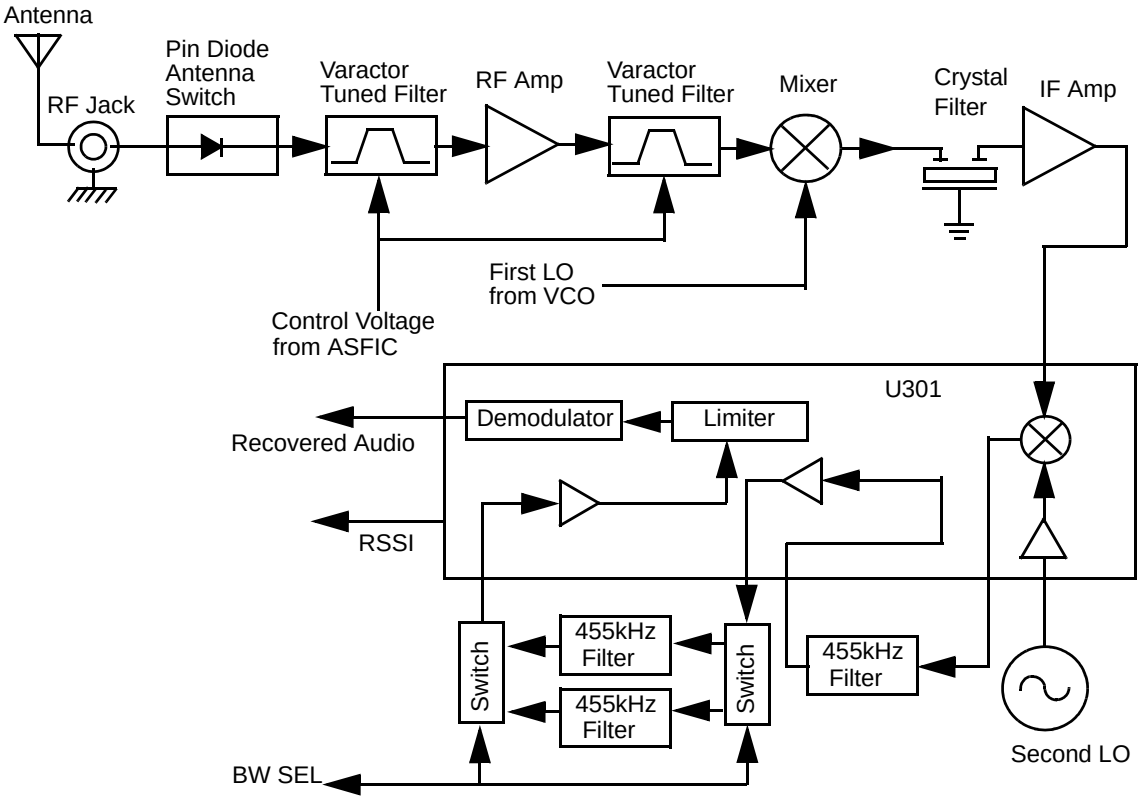

Figure 5-2. UHF Receiver Block Diagram

5.2.1 Receiver Front-End

(Refer to the *UHF Receiver Front End Schematic Diagram* on page 9-178 and the *UHF Transmitter Schematic Diagram* on page 9-183.

The RF signal is received by the antenna and applied to a low-pass filter. For UHF, the filter consists of L101, L102, C102, C103, C104. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes (CR101 and CR102) and a pi network (C106, L104 and C107).The signal is then applied to a varactor tuned bandpass filter. The UHF bandpass filter comprises L301, L302, C302, C303, C304, CR301, and CR302. The bandpass filter is tuned by applying a control voltage to the varactor diodes (CR301 and CR302) in the filter.

The bandpass filter is electronically tuned by the DACRx from IC404, which is controlled by the microprocessor. Depending on the carrier frequency, the DACRx will supply the tuned voltage to the varactor diodes in the filter. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q301 via C307. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L306, L307, C313, C317, CR304, and CR305.

Both the pre- and post-RF amplifier varactor tuned filters have similar responses. The 3 dB bandwidth of the filter is about 50 MHz. This enables the filters to be electronically controlled by using a single control voltage which is DACRx.

The output of the post-RF amplifier filter which is connected to the passive double balanced mixer consists of T301, T302, and CR306. Matching of the filter to the mixer is provided by C381. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to the 44.85 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL301) through a resistor pad and a diplexer (C322 and L310). Matching to the input of the crystal filter is provided by C324 and L311. The crystal filter provides the necessary selectivity and intermodulation protection.

5.2.2 Receiver Back-End

(Refer to the *UHF Receiver Back End Schematic Diagram* on page 9-179.)

The output of crystal filter FL301 is matched to the input of first IF amplifier transistor Q302 by L330. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The IF amplifier provides a gain of about 16 dB. The amplified first IF signal is then coupled into U301 (pin 1) via C360 and L332, which provides the matching for the first IF amplifier and U301.

Within U301, the first IF 44.85 MHz signal mixes with the 44.395 MHz second local oscillator (2nd LO) to produce the second IF signal at 455 kHz. The 2nd LO signal frequency is determined by crystal Y300. The second IF signal (455 kHz) is then filtered by an external ceramic filter FL302 before being amplified by the second IF amplifier within U301. Again, the signal is filtered by a second external ceramic filter FL303 or FL304, depending on the selected channel spacing. FL303 is used for 20/25 kHz channel spacing whereas FL304 is used for 12.5 kHz channel spacing. The simple circuit consisting of U302, CR312, CR313 and resistors R345, R360, R321, and R324 divert the second IF signal according to the BW_SEL line. The filtered output of the second IF signal is applied to the limiter input pin of U301.

The IF IC (U301) contains a quadrature detector using a ceramic phase-shift element (Y301) to provide audio detection. Internal amplification provides an audio output level around 120 mVrms (@60% deviation) from pin 8 of U301. This demodulated audio is fed to the ASFIC_CMP IC (U404) in the controller section.

The IF IC (U301) also performs several other functions. It provides a received signal-strength indicator (RSSI) with a dynamic range of 70 dB. The RSSI is a DC voltage monitored by the microprocessor, and is used as a peak indicator during the bench tuning of the receiver front-end varactor filter.

5.3 Frequency Generation Circuitry

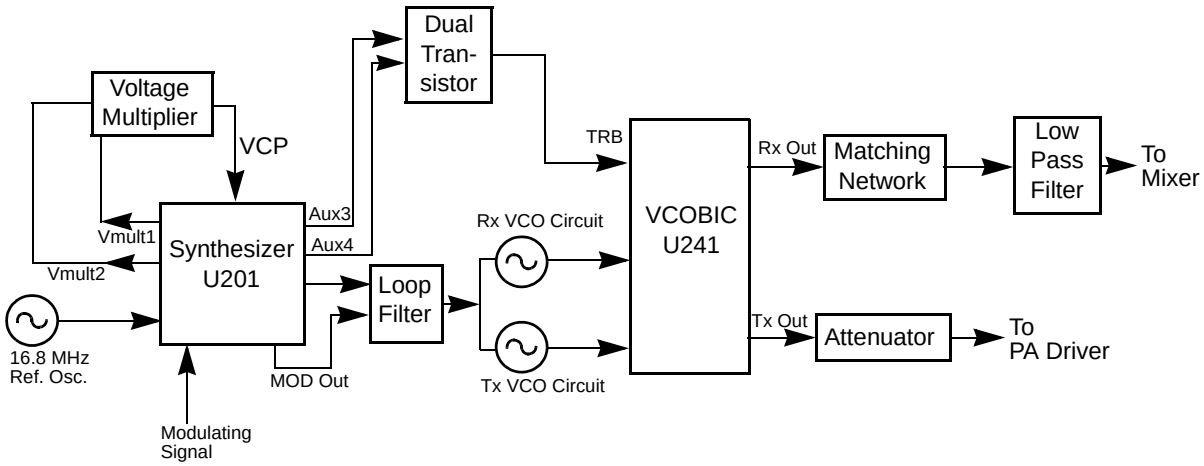

Figure 5-3. Frequency Generation Unit Block Diagram

The Frequency Generation Circuitry is composed of two main ICs:

- Fractional-N synthesizer (U201)
- VCO/Buffer IC (U241)

Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5 V and 3.3 V, which come from U247 and U248, respectively. The synthesizer in turn generates a superfiltered 4.5 V which powers U241.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3 V DC signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin 10 of U201. Internally, the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

5.4 Synthesizer

(Refer to the *UHF Synthesizer Schematic Diagram* on page 9-180.)

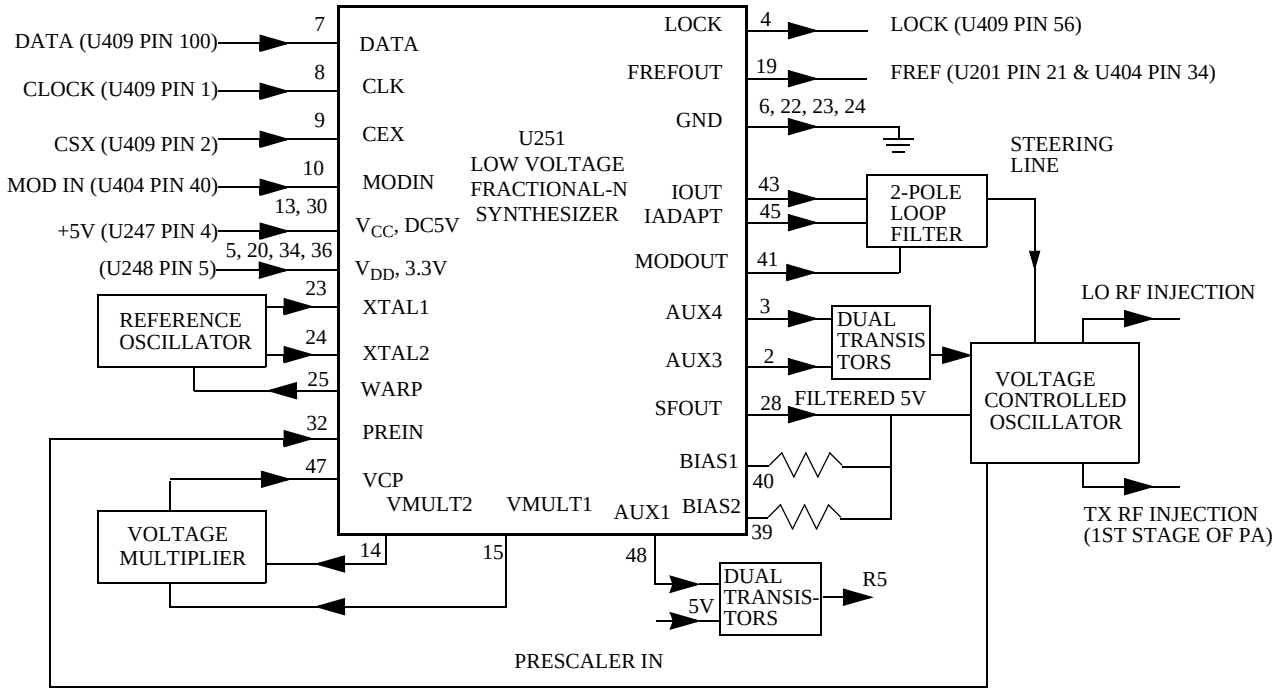

Figure 5-4. Synthesizer Block Diagram

The Fractional-N Synthesizer uses a 16.8 MHz crystal (FL201) to provide a reference for the system. The LVFractN IC (U201) further divides this to 2.1 MHz, 2.225 MHz, and 2.4 MHz as reference frequencies. Together with C206, C207, C208, R204, and CR203, they build up the reference oscillator which is capable of 2.5 ppm stability over temperatures of –30 to 85°C. It also provides 16.8 MHz at pin 19 of U201 to be used by ASFIC.

The loop filter, which consists of C231, C232, C233, R231, R232, and R233, provides the necessary DC steering voltage for the VCO and determines the amount of noise and spur passing through.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put the synthesizer within the lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier, which is made up of C258, C259, C228, triple diode CR201 and level shifters U210 and U211. Two 3.3 V square waves (180 deg out of phase) are first shifted to 5 V, then along with regulated 5 V, put through arrays of diodes and capacitors to build up 13.3 V at pin 47 of U201.

5.5 Voltage-Controlled Oscillator (VCO)

(Refer to the *UHF Voltage Controlled Oscillator Schematic Diagram* on page 9-181.

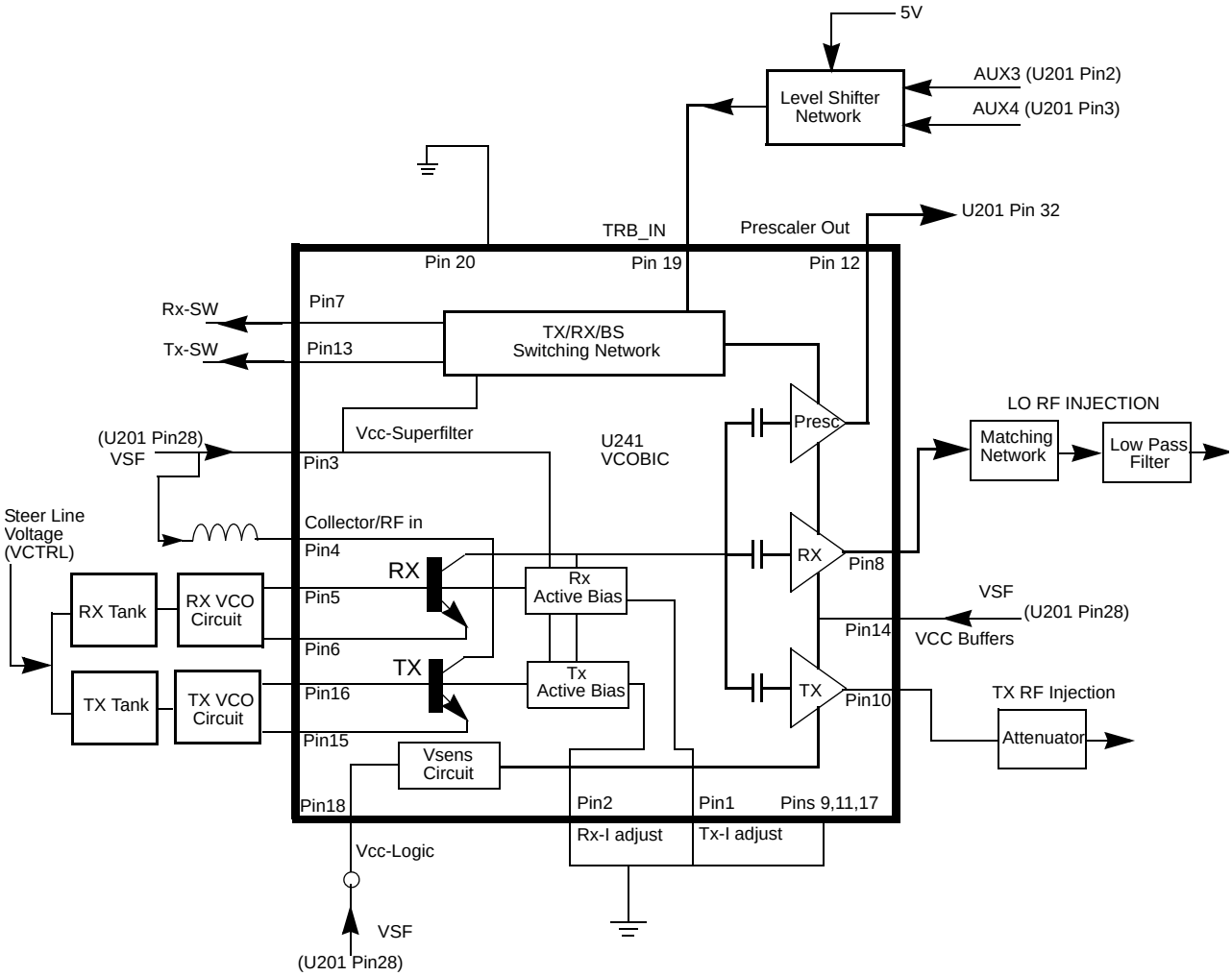

Figure 5-5. VCO Block Diagram

The VCOBIC (U241), in conjunction with the Fractional-N synthesizer (U201), generates RF in both the receive and the transmit modes of operation. The TRB line (U241 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U241 pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage between 3.5 V and 9.5 V when the PLL is locked on frequency.

The VCOBIC (U241) is operated at 4.54 V (VSF) and Fractional-N synthesizer (U201) at 3.3 V. This difference in operating voltage requires a level shifter consisting of Q260 and Q261 on the TRB line.

The operation logic is shown in Table 5-1.

Table 5-1. Level Shifter Logic

Desired Mode	AUX 4	AUX 3	TRB
Tx	Low	High (@3.2V)	High (@4.8V)
Rx	High	Low	Low
Battery Saver	Low	Low	Hi-Z/Float (@2.5V)

In the receive mode, U241 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U241. The RF signal at U241 pin 8 is run through a matching network. The resulting RF signal is the LO RF INJECTION, and it is applied to the mixer at T302 (refer to the *UHF Receiver Front End Schematic Diagram* on page 9-178).

During the transmit condition, when PTT is depressed, five volts is applied to U241 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U241. The RF signal at U241 pin 10 is injected into the input of the PA module (U101 pin16). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through the U201 pin 41.

When a high impedance is applied to U241 pin 19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

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Chapter 6 VHF Theory of Operation

6.1 Transmitter

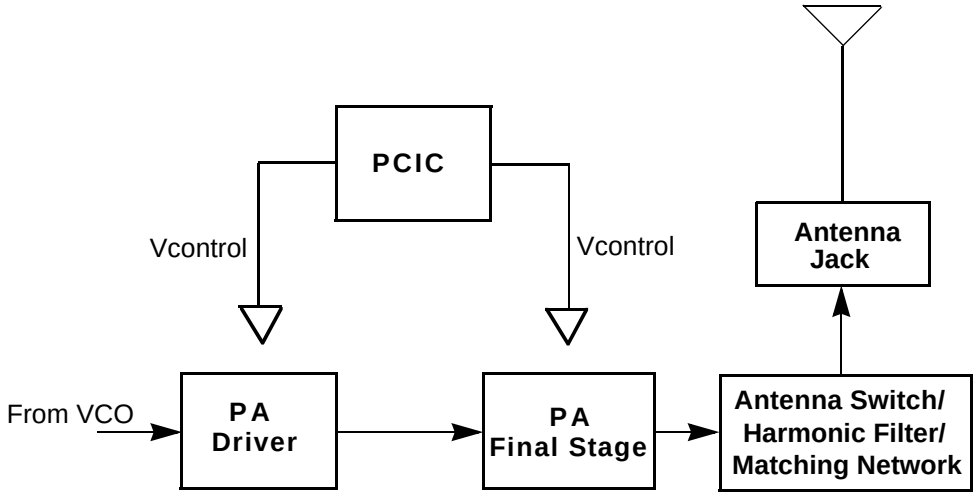


Figure 6-1. Transmitter Block Diagram

6.1.1 General

(Refer to Figure 6-1.)

The VHF transmitter contains five basic circuits:

- Power amplifier
- Antenna switch
- Harmonic filter
- Antenna matching network
- Power control integrated circuit (PCIC)

6.1.2 Power Amplifier

The power amplifier consists of two devices:

- 9Z67 LDMOS driver IC (U3501)
- PRF1507 LDMOS PA (Q3501)

The 9Z67 LDMOS driver IC contains a two-stage amplification with a supply voltage of 7.3 V.

This RF power amplifier is capable of supplying an output power of 0.3 W (pin 6 and 7) with an input signal of 2 mW (3 dBm) (pin16). The current drain would typically be 130 mA while operating in the frequency range of 136-174 MHz.

The PRF1507 LDMOS PA is capable of supplying an output power of 7 W with an input signal of 0.3W. The current drain would typically be 1800 mA while operating in the frequency range of 136-174 MHz. The power output can be varied by changing the biasing voltage.

6.1.3 Antenna Switch

The antenna switch circuit consists of two PIN diodes (D3521 and D3551), a pi network (C3531, L3551 and C3550), and three current limiting resistors (R3571, R3572, R3573). In the transmit mode, B+ at PCIC (U3502) pin 23 will go low and turn on Q3561 where a B+ bias is applied to the antenna switch circuit to bias the diodes “on.” The shunt diode (D3551) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

6.1.4 Harmonic Filter

The harmonic filter consists of C3532 to C3536, L3531 and L3532. This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. The harmonic filter insertion loss should be less than 1.2 dB.

6.1.5 Antenna Matching Network

A matching network which is made up of L3538 and C3537 is used to match the antenna's impedance to the harmonic filter. This will optimize the performance of the transmitter and receiver into an antenna.

6.1.6 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U3502 to control the power output of the radio by maintaining the radio current drain. The current to the final stage of the power module is supplied through R3519 (0.1ohms), which provides a voltage proportional to the current drain. This voltage is then fed back to the Automatic Level Control (ALC) within the PCIC to keep the whole loop stable.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The voltage level is controlled by the microprocessor through the data line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C3562, C3563 and C3565) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

U3503 and its associated circuitry acts as a temperature cut back circuitry. This circuitry provides the necessary voltage to the PCIC to cut the transmitter power when the radio temperature gets too high.

6.2 Receiver (for all models except those with PCB 8486473Z04)

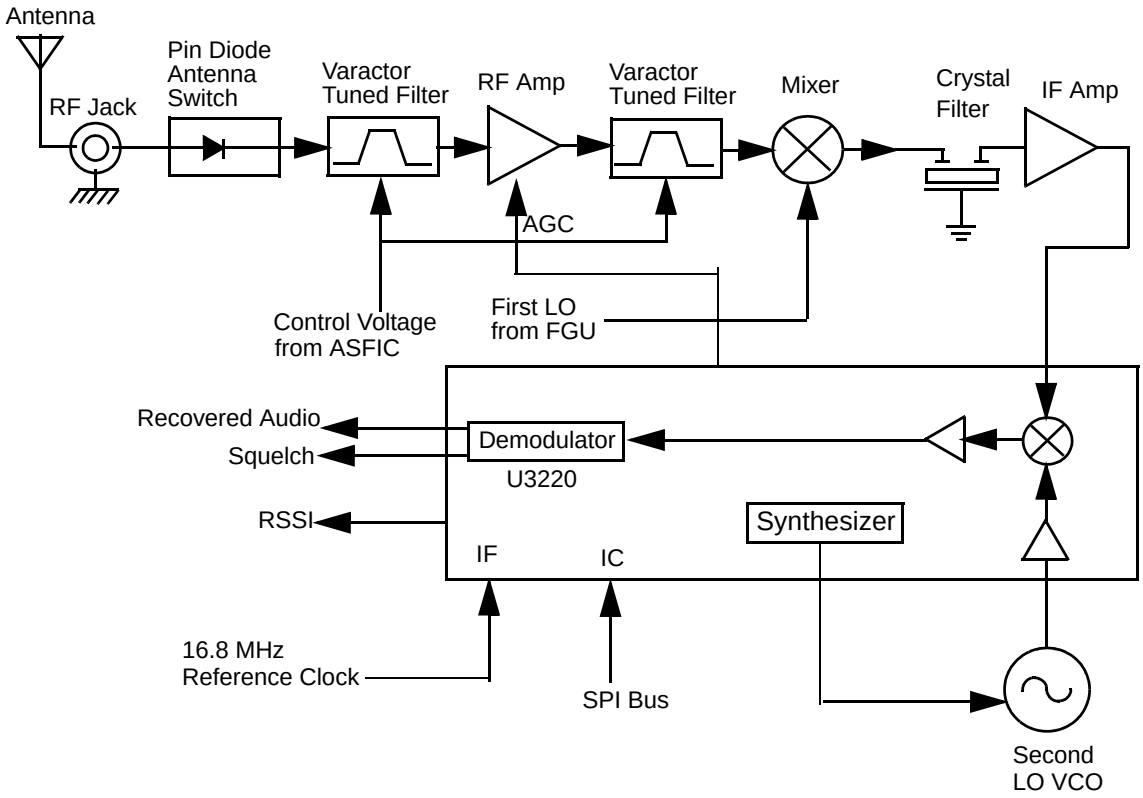


Figure 6-2. VHF Receiver Block Diagram

6.2.1 Receiver Front-End

(Refer to *VHF Receiver Front End Schematic Diagram* on page 9-78, *VHF Receiver Back End Schematic Diagram* on page 9-79, and *VHF Transmitter Schematic Diagram* on page 9-82).

The RF signal is received by the antenna and applied to a low-pass filter. For VHF, the filter consists of L3531, L3532, C3532 to C3563. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes(D3521 and D3551) and a pi network (C3531, L3551 and C3550).The signal is then applied to a varactor tuned bandpass filter. The VHF bandpass filter comprises of L3301, L3303, C3301 to C3304 and D3301. The bandpass filter is tuned by applying a control voltage to the varactor diode (D3301) in the filter.

The bandpass filter is electronically tuned by the DACRx from IC404 which is controlled by the microprocessor. Depending on the carrier frequency, the DACRx will supply the tuned voltage to the varactor diodes in the filter. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q3302 via C3306. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L3305, L3306, C3311 to C3314 and D3302.

Both the pre and post-RF amplifier varactor tuned filters have similar responses. The 3 dB bandwidth of the filter is about 12 MHz. This enables the filters to be electronically controlled by using a single control voltage which is DACRx.

The output of the post-RF amplifier filter is connected to the passive double balanced mixer which consists of T3301, T3302 and CR3301. Matching of the filter to the mixer is provided by C3317, C3318 and L3308. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using high side injection, the RF signal is down-converted to the 45.1 MHz IF signal.

The IF signal coming out of the mixer is transfered to the crystal filter (Y3200) through a resistor pad (R3321 - R3323) and a diplexer (C3320 and L3309). Matching to the input of the crystal filter is provided by C3200 and L3200. The crystal filter provides the necessary selectivity and intermodulation protection.

6.2.2 Receiver Back-End

(Refer to *VHF Receiver Back End Schematic Diagram* on page 9-79).

The output of crystal filter Y3200 is matched to the input of IF amplifier transistor Q3200 by capacitor C3203. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The gain controlled IF amplifer provides a maximum gain of about 10dB. The amplified IF signal is then coupled into U3220 (pin 3) via L3202, C3207, and C3230 which provides the matching for the IF amplifier and U3220.

The IF signal applied to pin 3 of U3220 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 27 of U3220. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in the IF module (U3220).

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U3220 so that it is very close to the first IF frequency. The IF IC (U3220) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO will “search” for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q3270. The VCO has a varactor diode, D3270, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C3278 to C3280, R3274 and R3275.

The IF IC (U3220) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used as a peak indicator during the bench tuning of the receiver front-end varactor filter. The RSSI voltage is also used to control the automatic gain control (AGC) circuit at the front-end.

The demodulated signal on pin 27 of U3220 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

6.2.3 Automatic Gain Control Circuit

(Refer to *VHF Receiver Front End Schematic Diagram* on page 9-78 and *VHF Receiver Back End Schematic Diagram* on page 9-79).

The front end automatic gain control circuit provides automatic reduction of gain, of the front end RF amplifier via feedback. This action is necessary to prevent overloading of backend circuits. This is achieved by drawing some of the output power from the RF amplifier output. At high radio frequencies, capacitor C3327 provides the low impedance path to ground for this purpose. CR3302 is a PIN diode used for switching the path on or off. A certain amount of forward biasing current is needed to turn the PIN diode on. Transistor Q3301 provides this current.

Radio signal strength indicator, RSSI, a voltage signal, is used to drive Q3301 to saturation i.e. turned on. RSSI is produced by U3220 and is proportional to the gain of the RF amplifier and the input power to the radio.

Resistors R3304 and R3305 are voltage dividers designed to turn on Q3301 at certain RSSI levels. In order to turn on Q3301 the voltage across R3305 must be greater or equal to the voltage across R3324, plus the base-emitter voltage (Vbe) present at Q3301. Capacitor C3209 is used to dampen any instability while the AGC is turning on. The current flowing into the collector of Q3301, a high current gain NPN transistor, will be drawn through the PIN diode to turn it on. Maximum current flowing through the PIN is limited by the resistors R3316, R3313, R3306 and R3324. C3326 is a feedback capacitor used to provide some stability to this high gain stage.

An additional gain control circuit is formed by Q3201 and its associated circuitry. Resistors R3206 and R3207 are voltage dividers designed to turn on Q3201 at a significantly higher RSSI level than the level required to turn on PIN diode control transistor Q3301. In order to turn on Q3201 the voltage across R3207 must be greater or equal to the voltage across R3208, plus the base-emitter voltage (Vbe) present at Q3201. As current starts flowing into the collector of Q3201, it reduces the bias voltage at the base of IF amplifier transistor Q3200 and in turn, the gain of the IF amplifier. The gain can be controlled in a range of -30 dB up to +10 dB.

6.3 Receiver (for models with PCB 8486473Z04)

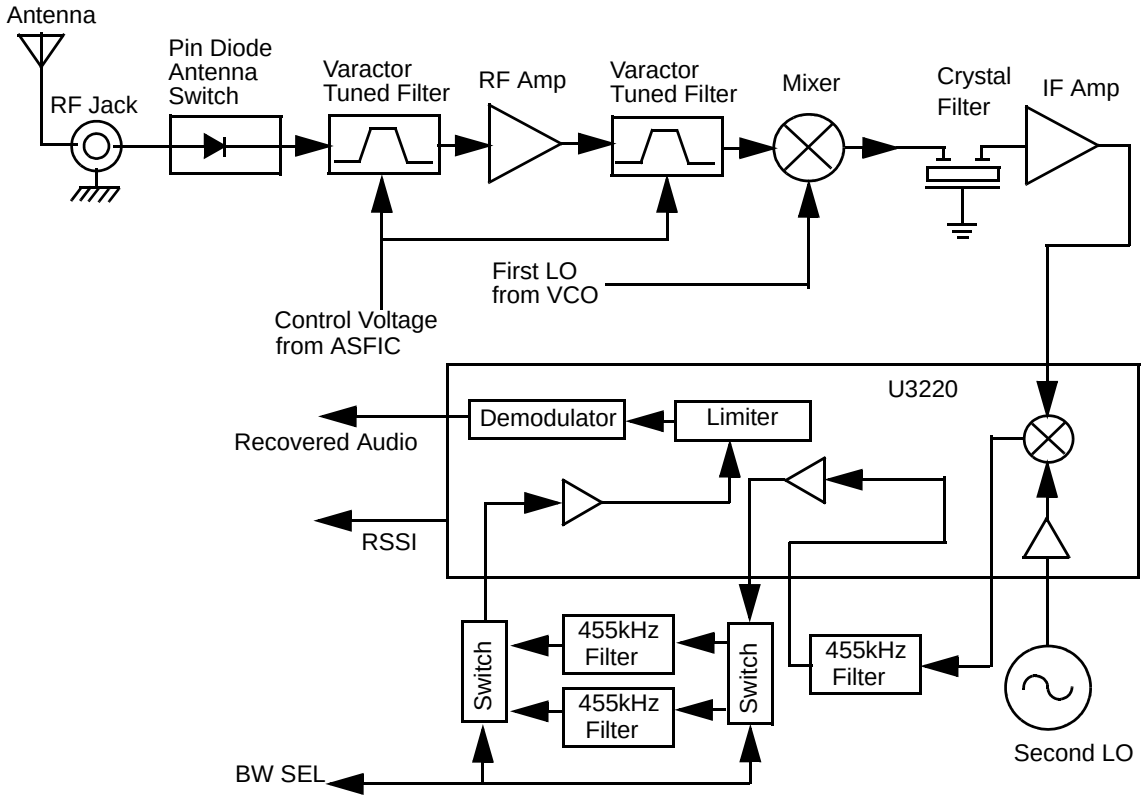


Figure 6-3. VHF Receiver Block Diagram

6.3.1 Receiver Front-End

(Refer to *VHF Receiver Front-End Schematic Diagram* on page 9-92, *VHF Receiver Back-End Schematic Diagram* on page 9-93, and *VHF Transmitter Schematic Diagram* on page 9-96.)

The RF signal is received by the antenna and applied to a low-pass filter. For VHF, the filter consists of L3531, L3532, C3532 to C3563. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes (D3521 and D3551) and a pi network (C3531, L3551 and C3550).The signal is then applied to a varactor tuned bandpass filter. The VHF bandpass filter comprises of L3301, L3303, C3301 to C3304 and D3301. The bandpass filter is tuned by applying a control voltage to the varactor diode (D3301) in the filter.

The bandpass filter is electronically tuned by the DACRx from IC404 which is controlled by the microprocessor. Depending on the carrier frequency, the DACRx will supply the tuned voltage to the varactor diodes in the filter. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q3302 via C3306. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L3305, L3306, C3311 to C3314 and D3302.

Both the pre and post-RF amplifier varactor tuned filters have similar responses. The 3 dB bandwidth of the filter is about 12 MHz. This enables the filters to be electronically controlled by using a single control voltage which is DACR*x*.

The output of the post-RF amplifier filter is connected to the passive double balanced mixer which consists of T3301, T3302 and CR3301. Matching of the filter to the mixer is provided by C3317, C3318 and L3308. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using high side injection, the RF signal is down-converted to the 44.85 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (Y3200) through a resistor pad (R3321 - R3323) and a diplexer (C3320 and L3309). Matching to the input of the crystal filter is provided by C3201 and L3200. The crystal filter provides the necessary selectivity and intermodulation protection.

6.3.2 Receiver Back-End

(Refer to *VHF Receiver Back-End Schematic Diagram* on page 9-93.)

The output of crystal filter Y3200 is matched to the input of IF amplifier transistor Q3200 by L3203. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The IF amplifier Q3200 is actively biased by a collector base feedback provided by R3202 and R3203. The gain controlled IF amplifer provides a maximum gain of about 16dB. A dual hot carrier diode (CR3201) limits the filter output voltage swing to reduce overdrive effects at RF levels above -27dBm. The amplified IF signal is then coupled into U3220 (pin 1) via L3202, C3207, and C3200 which provides the matching for the IF amplifier and U3220.

The IF signal applied to pin 1 of U3220 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 7 of U3220.

Within U3220, the first IF 44.85 MHz signal mixes with the 44.395 MHz second local oscillator (2nd LO) to produce the second IF signal at 455 kHz. The 2nd LO signal frequency is determined by crystal Y3201. The second IF signal (455 kHz) is then filtered by an external ceramic filter Y3205 before being amplified by the second IF amplifier within U3220. Again, the signal is filtered by a second external ceramic filter Y3203 or Y3204 depending on the selected channel spacing. Y3203 is used for 20/25 kHz channel spacing whereas Y3204, for 12.5 kHz channel spacing. The simple circuit consisting of U3221, CR3202, CR3203 and resistors R3209, R3212, R3211 and R3205 divert the second IF signal according to the BW_SEL line. The filtered output of the second IF signal is applied to the limiter input pin of U3220 (Pin 14).

The IF IC (U3220) contains a quadrature detector using a ceramic phase-shift element (Y3202) to provide audio detection. Internal amplification provides an audio output level around 120mVrms (@60% deviation) from pin 8 of U3220. This demodulated audio is fed to the ASFIC_CMP IC (U404) in the controller section.

The IF IC (U3220) also performs several other functions. It provides a received signal-strength indicator (RSSI) with a dynamic range of 70 dB. The RSSI is a dc voltage monitored by the microprocessor, and used as a peak indicator during the bench tuning of the receiver front-end varactor filter.

6.3.3 Automatic Gain Control Circuit

(Refer to *VHF Receiver Front-End Schematic Diagram* on page 9-92 and *VHF Receiver Back-End Schematic Diagram* on page 9-93.)

The front-end automatic gain control circuit provides automatic reduction of gain, of the front-end RF amplifier via feedback. This action is necessary to prevent overloading of back-end circuits. This is achieved by drawing some of the output power from the RF amplifier output. At high radio frequencies, capacitor C3327 provides the low impedance path to ground for this purpose. CR3302 is a PIN diode used for switching the path on or off. A certain amount of forward biasing current is needed to turn the PIN diode on. Transistor Q3301 provides this current.

Radio signal strength indicator, RSSI, a voltage signal, is used to drive Q3301 to saturation i.e. turned on. RSSI is produced by U3220 and is proportional to the gain of the RF amplifier and the input power to the radio.

Resistors R3304 and R3305 are voltage dividers designed to turn on Q3301 at certain RSSI levels. In order to turn on Q3301 the voltage across R3305 must be greater or equal to the voltage across R3324, plus the base-emitter voltage (Vbe) present at Q3301. Capacitor C3209 is used to dampen any instability while the AGC is turning on. The current flowing into the collector of Q3301, a high current gain NPN transistor, will be drawn through the PIN diode to turn it on. Maximum current flowing through the PIN is limited by the resistors R3316, R3313, R3306 and R3324. C3326 is a feedback capacitor used to provide some stability to this high gain stage.

An additional gain control circuit is formed by Q3201 and its associated circuitry. Resistors R3206 and R3207 are voltage dividers designed to turn on Q3201 at a significantly higher RSSI level than the level required to turn on PIN diode control transistor Q3301. In order to turn on Q3201 the voltage across R3207 must be greater or equal to the voltage across R3208, plus the base-emitter voltage (Vbe) present at Q3201. As current starts flowing into the collector of Q3201, it reduces the bias voltage at the base of IF amplifier transistor Q3200 and in turn, the gain of the IF amplifier. The gain can be controlled in a range of -30 dB up to +10 dB.

6.4 Frequency Generation Circuitry

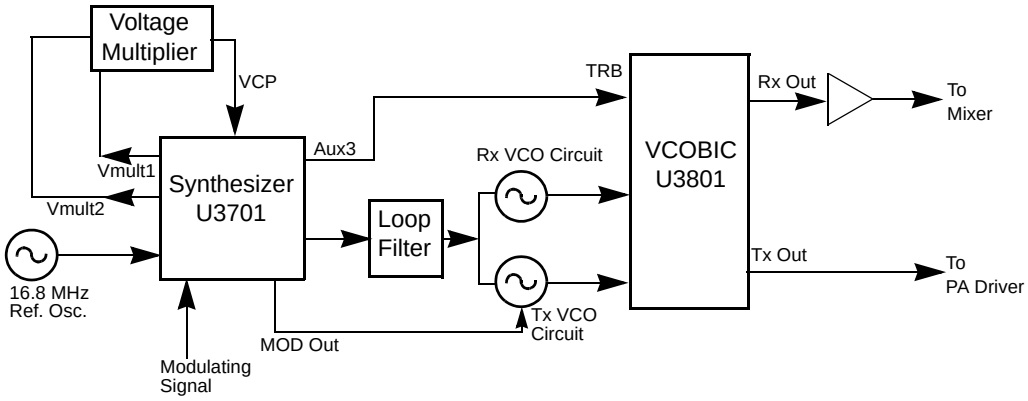


Figure 6-4. Frequency Generation Unit Block Diagram

The Frequency Generation Circuitry is composed of two main ICs, the Fractional-N synthesizer (U3701), and the VCO/Buffer IC (U3801). Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5 V and 3.3 V which come from U3711 and U3201 respectively. The synthesizer in turn generates a superfiltered 4.5 V which powers U3801.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3 V dc signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U3701. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

6.5 Synthesizer

(Refer to the *VHF Synthesizer Schematic Diagram* on page 9-94.)

The Fractional-N Synthesizer uses a 16.8MHz crystal (Y3761) to provide a reference for the system. The LVFractN IC (U3701) further divides this to 2.1MHz, 2.225 MHz, and 2.4 MHz as reference frequencies. Together with C3761, C3762, C3763, R3761 and D3761, they build up the reference oscillator which is capable of 2.5ppm stability over temperatures of -30 to 85°C. It also provides 16.8 MHz at pin 19 of U3701 to be used by ASFIC.

The loop filter which consist of C3721, C3722, R3721, R3722 and R3723 provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U3701 to put synthesizer within the lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier which is made up of C3701 to C3704 and triple diodes D3701, D3702. Two 3.3 V square waves (180 deg out of phase) are first multiplied by four and then shifted, along with regulated 5 V, to build up 13.5 V at pin 47 of U3701.

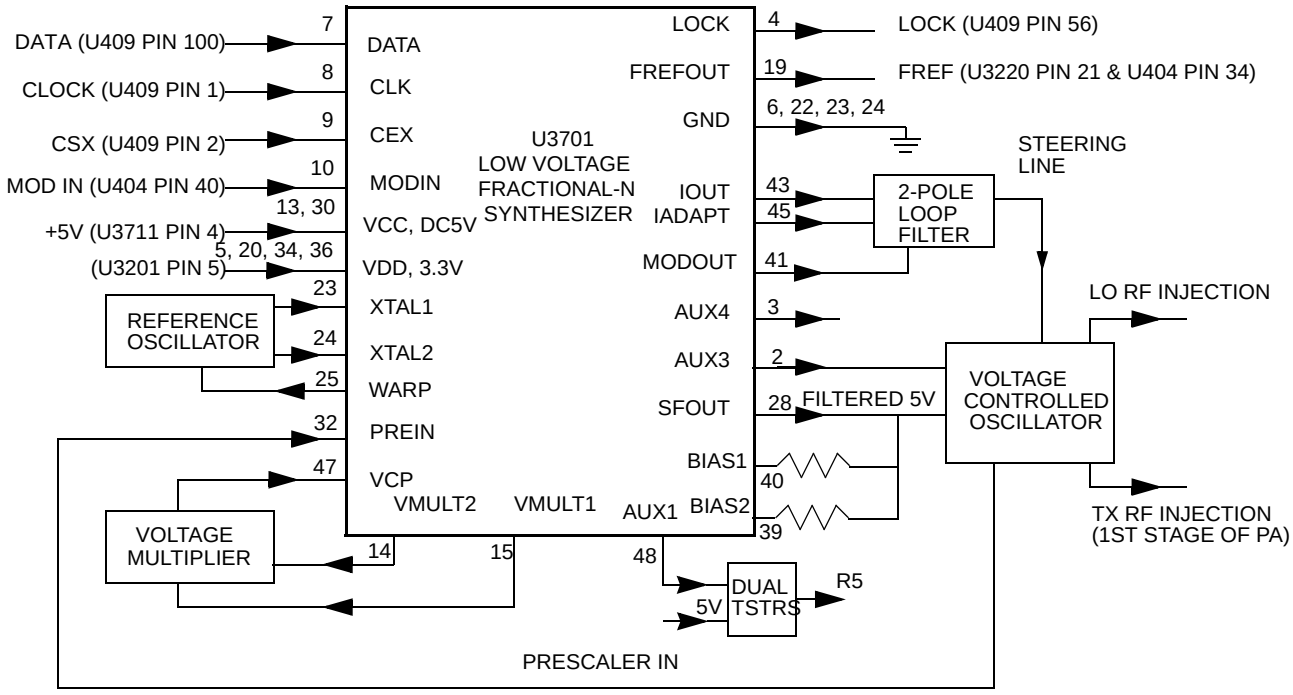


Figure 6-5. Synthesizer Block Diagram

6.6 Voltage-Controlled Oscillator (VCO)

(Refer to the *VHF Voltage-Controlled Oscillator Schematic Diagram* on page 9-95.)

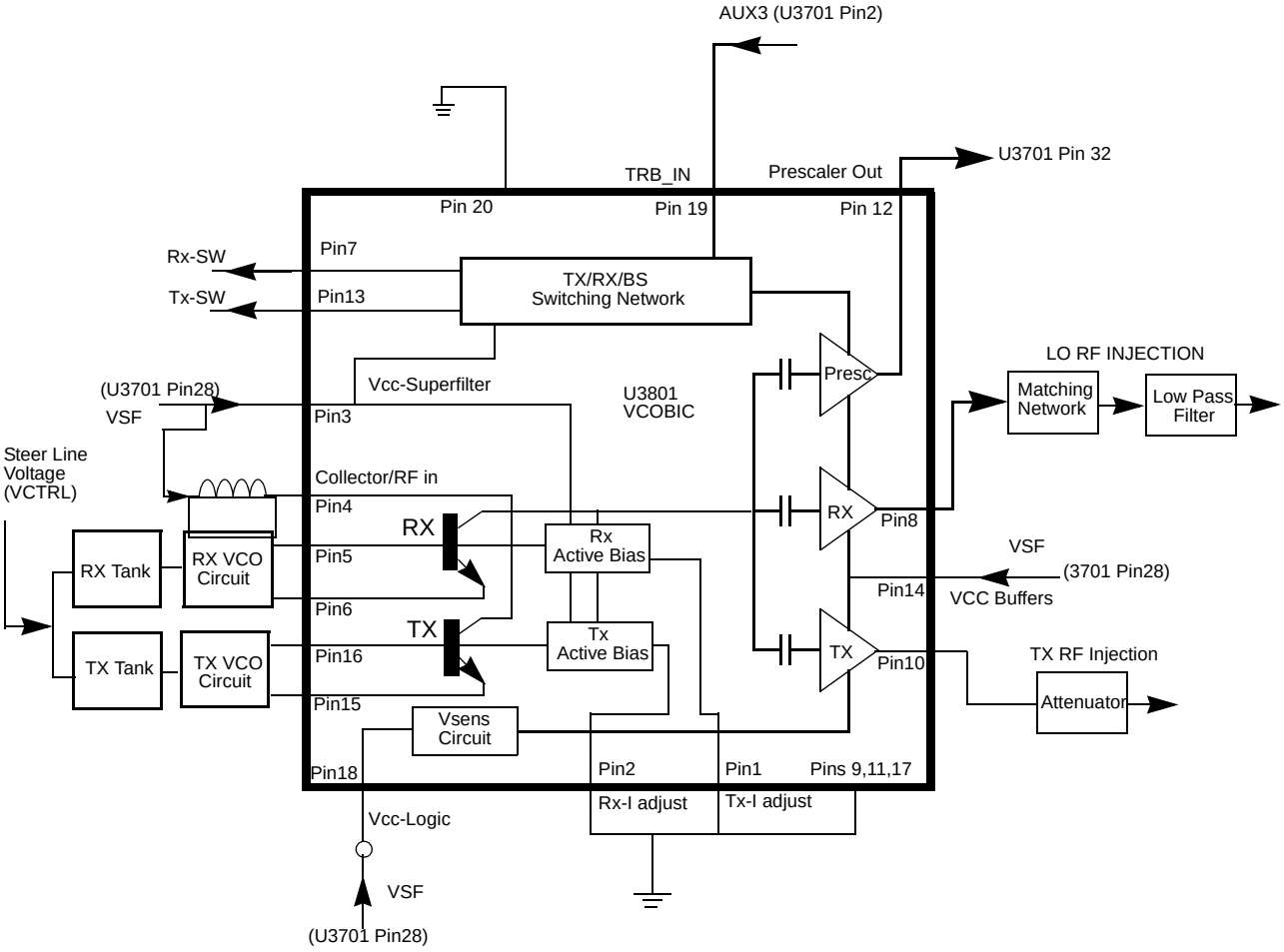


Figure 6-6. VCO Block Diagram

The VCOBIC (U3801) in conjunction with the Fractional-N synthesizer (U3701) generates RF in both the receive and the transmit modes of operation. The TRB line (U3801 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U3801 pin 12, through a low pass filter, to the prescaler input (U3701 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage typically between 3.5 V and 9.5 V when the PLL is locked on frequency.

The RF section of the VCOBIC(U3801) is operated at 4.54 V (VSF), while the control section of the VCOBIC and Fractional-N synthesizer (U3701) is operated at 3.3 V. The operation logic is shown in Table 6-1.

Table 6-1. VCO Control Logic

Desired Mode	AUX 4	AUX 3	TRB
Tx	n.u.	High (@3.2V)	High (@3.2V)
Rx	n.u.	Low	Low
Battery Saver	n.u.	Hi-Z/Float (@1.6V)	Hi-Z/Float (@1.6V)

In receive mode, U3801 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U3801. The RF signal at U3801 pin 8 is run through a matching network. The resulting RF signal is the LO RF INJECTION and it is applied to the mixer at T3302.

During the transmit condition, when PTT is depressed, 3.2 volts is applied to U3801 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U3801. The RF signal at U3801 pin 10 is injected into the input of the PA module (U3501 pin16). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through U3701 pin 41.

When a high impedance is applied to U3801 pin 19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

Chapter 7 Low Band, 800 MHz, PassPort & 900 MHz Theory of Operation

7.1 Introduction

This chapter provides a detailed theory of operation for the radio components. Schematic diagrams for the circuits described in the following paragraphs are located in Figures 9-238 through 9-284.

7.2 Low Band Transmitter

The low band transmitter consists of the following basic circuits as shown in Figure 7-1.

- Power amplifier (PA).
- Antenna switch/harmonic filter.
- Antenna matching network.
- Power control integrated circuit (PCIC).

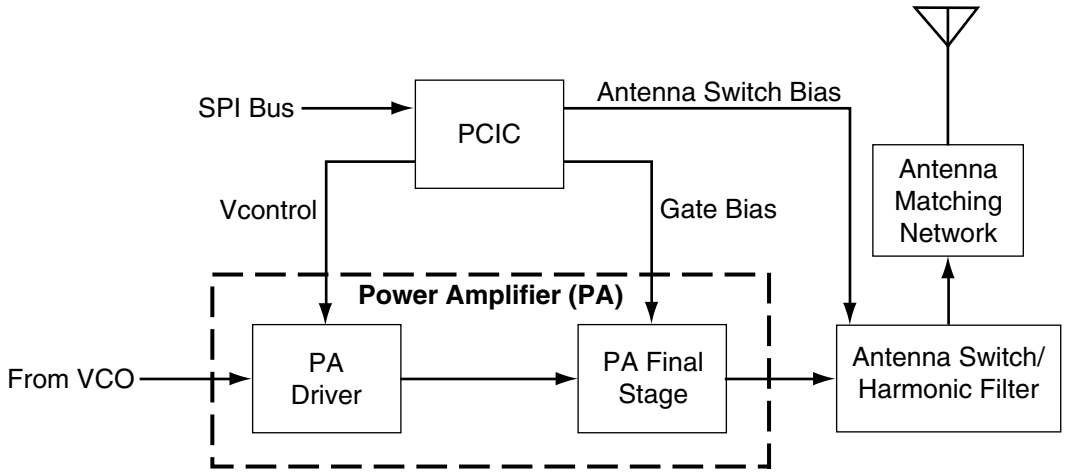


Figure 7-1. Low Band Transmitter Block Diagram

7.2.1 Power Amplifier (PA)

The PA consists of two LDMOS devices:

- PA driver, U101.
- PA final stage, Q100.

The LDMOS driver (U101) provides 2-stage amplification using a supply voltage of 7.3V. The amplifier is capable of supplying an output power of 0.3 W (pins 6 and 7) with an input signal of 2mW at (pin16). The current drain is typically 120 mA while operating in the frequency range of 29.7 - 50 MHz. The power output of this stage is varied by the power control loop which controls the voltage on pin 1.

The LDMOS PA is capable of supplying an output power of 8W with an input signal of 0.3 W. The current drain is typically 2000 mA while operating in the frequency range of 29.7 - 50 MHz. The final stage gate is bias by a voltage from PCIC, pin 24. This voltage is the output of a programmable DAC inside the PCIC and the output is adjustable with the radio tuner.

7.2.2 Antenna Switch

The antenna switch circuit consists of two pin diodes (D100 and D101), a RF network (C147 and L103), and a DC feed network (L104, C144, and current limiting resistor R101). In the transmit mode, PCIC (U102) pin 32 goes high supplying current via the feed network to bias the diodes “on”. The shunt diode (D101) shorts out the receiver port and L103 is connected from the RF path to ground. L103 and the input capacitance of the lowpass filter form a parallel resonant circuit, effectively disconnecting the receiver port from the antenna while not loading the transmit path. In the receive mode, pin 32 goes low and the diodes are off. D100 looks like a high impedance effectively disconnecting the transmitter from the antenna while L103 and C147 form a series resonant circuit effectively connect the receiver to the antenna.

7.2.3 Harmonic Filter

The harmonic filter consists of components C103, C106, C103, C107,C110, C111, C114, C115 and inductors L100, L101, and L102 which are a part of the SH100 assembly. The harmonic filter for lowband is pole zero design. This feature gives greater attenuation in low frequencies where the harmonic energy of the transmitter is the greatest and less attenuation in high frequencies where there is less harmonic energy. The harmonic filter insertion loss is typically less than 0.8 dB.

7.2.4 Antenna Matching Transformer

The antenna matching transformer (T100) matches the antenna impedance with the harmonic filter to optimize the performance of the transmitter and receiver.

7.2.5 Power Control Integrated Circuit (PCIC)

The transmitter uses the PCIC (U102) to regulate the power output of the radio. To accomplish this, the voltage across R102 is sensed. This voltage drop is directly proportional to the current drawn in the final stage of the transmitter. This voltage is compared to a programmable reference inside the PCIC and the voltage on PCIC pin 4 adjusted. Pin 4 connects to the PA driver IC (U101) pin 1 via resistor R100 and varies RF output power of the driver. This controls the current drain of the final stage and sets the output power.

7.2.6 Temperature Cut Back Circuit

Temperature sensor VR101 and associated components are part of a temperature cut back circuit. This circuit senses the printed circuit board temperature around the transmitter circuits and outputs a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold of the PCIC, the transmitter output power decreases to reduce the transmitter temperature.

7.2.7 Electrostatic Discharge (ESD) Protection Circuit

The LDMOS PA device (Q100) is very sensitive to static discharge. To protect the device from ESD, a protection circuit consisting of single high-speed Schottky Diode (D104) is connected from the Antenna Nut (J102) to ground. This diode effectively shorts ESD energy to ground, but looks like an open circuit to normal RF energy. The diode turns on when the voltage at the antenna nut exceeds 150V.

7.3 Low Band Receiver

The low band receiver consists of a front end, back end, and automatic gain control circuits. A block diagram of the receiver is shown in Figure 7-2. Detailed descriptions of these stages are contained in the paragraphs that follow.

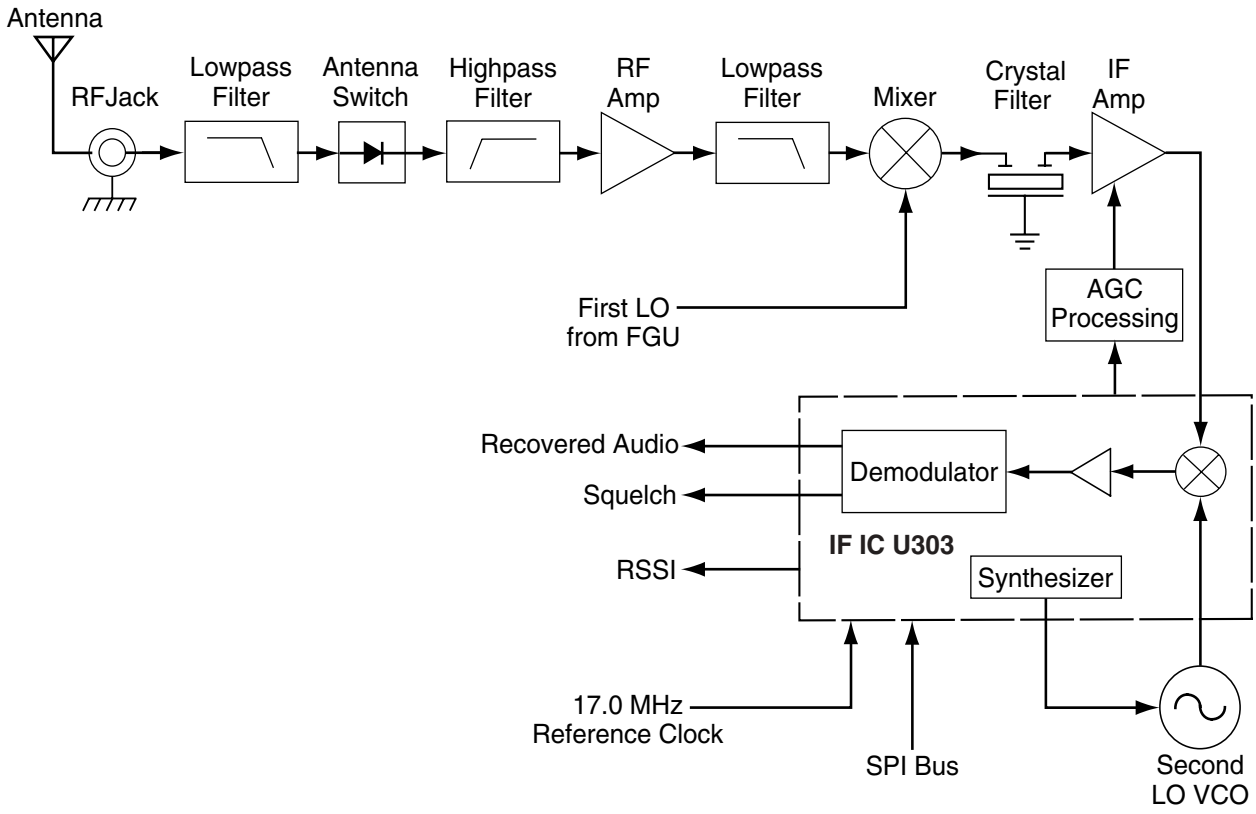


Figure 7-2. Low Band Receiver Block Diagram

7.3.1 Receiver Front-End

The RF signal received by the antenna is routed through the transmitter lowpass filter and antenna switch. These circuits are described in the transmitter section.The signal next passes through a highpass filter consisting of L501, L502, C538, C533 and C504. This filter serves to reject below band signals and has a 3 dB corner frequency of 27 MHz.

The output of the highpass filter is connected to an RF amp consisting of Q509 and associated biasing components. This is a BJT amplifier powered off 5 volts and has 13 dB of gain. The amplifier drives a lowpass filter consisting of L503, L504 L507, C534, C535, C536, C537 and C515. This filter is a pole zero design that filters off harmonic components from the RF amp. The 3 dB corner of this filter is at 56 MHz.

The output of the lowpass filter is connected to the passive double balanced mixer consisting of components T501, T502, and D501. After mixing with the first local oscillator up-converted to a 109.65 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL301) through a resistor pad (R507, R508 and R509) and a diplexer (C516 and L508). Matching to the input of the crystal filter is provided by L301, L302, C301 and C302. The 3 pole crystal filter provides the necessary selectivity and intermodulation protection.

7.3.2 Receiver Back-End

The output of crystal filter FL301 is connected to the input of IF amplifier transistor U301. Components L303 and C348 and R301 form the termination for the crystal filter and the signal is coupled to one gate of U301 by C303. The IF amplifier is a dual gate MOSFET powered off of the 5 volt supply. The first gate receives the IF signal as indicated previously. The second gate receives a DC voltage from U302 which serves as an AGC control signal. This signal reduces the gain of the IF amplifier to prevent overload of the IF IC, U303. The gain can be varied from a maximum of 13 dB to an attenuation of 55 dB. The output IF signal from U301 is coupled into U303 (pin 3) via C306, R304 and L304 which provides matching for the IF amplifier and U303.

The IF signal applied to pin 3 of U303 is amplified, down-converted, filtered, and demodulated, to produce recovered audio at pin 27 of U303. This IF IC is electronically programmable, and the amount of filtering, which is dependent on the radio channel spacing, is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in IF IC U303.

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U303 so that it is very close to the first IF frequency. The IF IC (U303) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO searches for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO locks onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q301. The VCO has a varactor diode, CR301, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of components C308, C309, and R310.

The IF IC (U303) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI voltage is also used to control the automatic gain control (AGC) circuit at the back end.

The demodulated signal on pin 27 of U303 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

7.3.3 Automatic Gain Control (AGC)

The automatic gain control circuit provides automatic reduction of gain to prevent overloading of backend circuits. This is achieved by lowering the voltage on one gate of U301 which will reduce the drain current in that part and lower its gain.

The Radio Signal Strength Indicator (RSS I) voltage signal for the IF IC (U303) is used to drive the AGC processing circuitry consisting of R306, R307, R308, R309 C307 and U302. As the received signal gets stronger, the RSSI line will rise. When the RSSI line passes a certain threshold, the voltage at the output of U302 will begin to drop. This voltage is connected to one gate of IF amplifier U301 through resistor R305. As this voltage decreases, it will lower the drain current in U301 and reduce the gain of the stage. This will limit the power incident on the IF IC, U303.

7.3.4 Frequency Generation Circuit

The frequency generation circuit, shown in Figure 7-3 on page 7-5, is composed of Low Voltage Fractional-N (LV FracN) synthesizer U205 and discrete RX VCO, TX VCO, and buffers as well as other supporting circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the schematic for the reference designators.

The synthesizer is powered by regulated 5V and 3.3 V. The 5 volt signal to the synthesizer as well as the rest of the radio is provided by U204. The 3.3 V signal is provided by U200 in the controller. The 5V signal goes to pins 13 and 30 while the 3.3 V signal goes to pins 5, 20, 34 and 36 of U201. The synthesizer in turn generates a superfiltered 4.3 V which powers the VCOs and buffers.

In addition to the VCO, the synthesizer also interfaces with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines (pins 7, 8 and 9) from the microprocessor, U409. A 3.3 V dc signal from pin 4 indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U205. Internally the audio is digitized by the LV FracN IC and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out at pin 41 to the VCO.

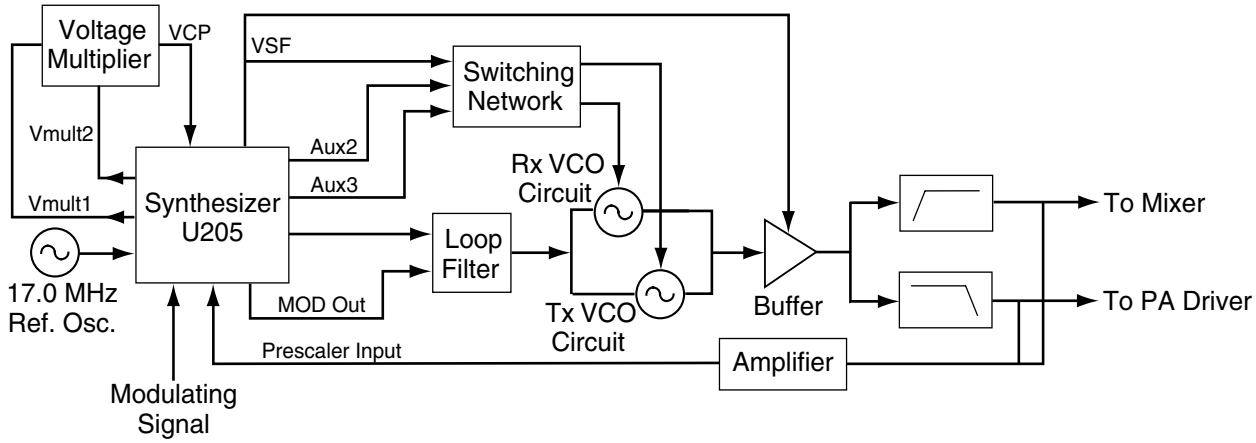


Figure 7-3. Low Band Frequency Generation Unit Block Diagram

7.4 Synthesizer

The Low Voltage Fractional-N (LV FracN) synthesizer, shown in Figure 7-4 on page 7-6, uses a 17.0 MHz crystal (Y201) to provide a reference for the system. Along with being used in the LV FracN synthesizer, the 17.0 MHz signal is provided at pin 19 of U205 for use by the ASFIC and LVZIF.

The LV FracN IC (U205) further divides this by 8 internally to give 2.125 MHz to be used as the reference frequency in the frequency synthesis. While UHF and VHF can use other references, (divide by 7 or divide by 7/8), only the divide by 8 function is valid for lowband.

The internal oscillator device in the LV FracN IC together with C236, C237, C242, R219, CR211and Y201 comprise the reference oscillator. This oscillator is temperature compensated is capable of 2.5 ppm stability over temperatures of -30° to 85°C. There is temperature compensation information that is unique to each crystal contained on Y201 that is programmed into the radio when built.

The loop filter consists of components C256, C257, C259, R224, R225 and R228. This circuit provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

To achieve fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U205 to put the synthesizer within lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C247, C283, C284, C285, C286, and triple diodes D210 and D211. This circuit provides 13.3V at U205, pin 47.

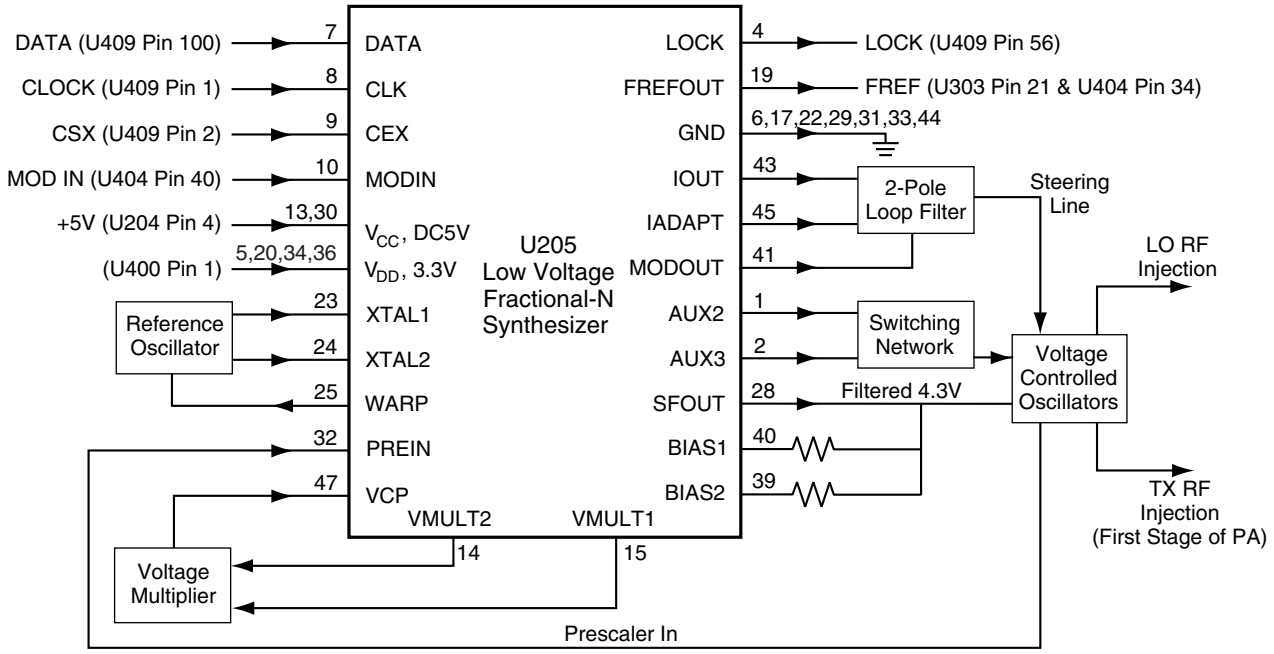


Figure 7-4. Low Band Synthesizer Block Diagram

7.5 Voltage Control Oscillators (VCO)

7.5.1 Receive VCO

The receive VCO is a Colpitts type design and using two active devices in parallel, Q202 and Q204. The oscillator is powered off of the 4.3 volt super filter supply when the AUX3 line goes low. The oscillator operates from 139 to 152 MHz for range 1 and 145 to 160 MHz for range 2. The frequency is tuned by varactor diodes CR201 and CR202.

7.5.2 Transmit VCO

The transmit VCO is a Hartley-type design with active devices Q203. The oscillator is powered off of the 4.3 volt super filter supply when the AUX2 line goes low. The oscillator operates from 29.7 to 42 MHz for Range 1 and 35 to 50 MHz for Range 2. The frequency is tuned by varactor diodes in U203. Note that the values of the inductive tap, L208 and L209, and the capacitor C215 which couples the varactor to the oscillator tank vary between the ranges.

7.5.3 Buffer

Both the receive and transmit VCO are fed to a buffer amplifier Q201. This is a BJT amplifier that boosts the signal levels to +4 dBm and provides reverse isolation to the oscillators. The amplifier is powered off the 4.3 volt super filter supply and the feed network is combined with the transmit filter.

7.5.4 Diplexer/Output Filters

The output of the buffer drives a pair of parallel filters forming a diplexer. One filter is a lowpass filter in the TX pass that passes 29.7 - 50 MHz signals for the transmitter into the power amplifier while rejecting the receive LO injection signals at 139 - 160 MHz. This filter is comprised of L204, L211, L212, C230 and C231.

The other filter is a highpass filter which passes 139 - 160 MHz signals for the receive LO into the mixer while rejecting the transmit injection signals at 29.7 -50 MHz. This filter is comprised of C228, C229, C235 and L215.

7.5.5 Prescalar Feedback

The prescalar input signal for receive and transmit is tapped off of the outputs of each filter by resistors R234 and R238. This signal is routed to the buffer amplifier consisting of components C287, Q288, R287, R288, and R289. The output of this buffer feeds U205, pin 32. After frequency comparison in the synthesizer, current is transferred in the loop filter and a control voltage is generated at the output of the loop filter to adjust the frequency of the VCO. This voltage is a DC voltage between 3.5V and 9.5V when the PLL is locked on frequency.

7.6 800 MHz Transmitter

The 800 MHz transmitter contains four basic circuits as shown in Figure 7-5:

- Power Amplifier (PA)
- Antenna Switch
- Harmonic Filter
- Power Control Integrated Circuit (PCIC).

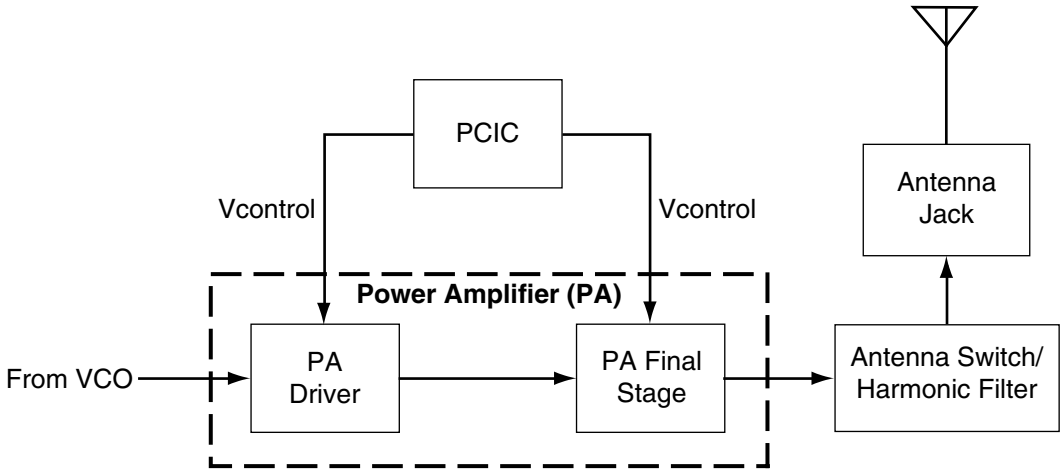


Figure 7-5. 800 MHz Transmitter Block Diagram

7.6.1 Power Amplifier

The power amplifier consists of two devices:

- 63J66 driver IC (U101) and
- 85Y73 LDMOS PA (Q101).

The 63J66 driver IC contains a 2 stage amplification with a supply voltage of 7.5V.

This RF driver IC is capable of supplying an output power of 0.3 W (pin 13 and 14) with an input signal of 2.5 mW (4 dBm) (pin16). The current drain would typically be 200 mA while operating in the frequency range of 806-870 MHz.

The 85Y73 LDMOS PA is capable of supplying an output power of 4.5 W with an input signal of 0.3W. The current drain would typically be 1100 mA while operating in the frequency range of 806-870 MHz. The power out can be varied by changing the biasing voltage and the drive level from the driver IC.

7.6.2 Antenna Switch

The antenna switch circuit consists of two PIN diodes (CR101 and CR102), a pi network (C109, L103 and C110), and three current limiting resistors (R101, R102, R103). In the transmit mode, B+ at PCIC (U102) pin 32 will go high, applying a B+ bias to the antenna switch circuit to bias the diodes “on”. The shunt diode (CR102) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

7.6.3 Harmonic Filter

The harmonic filter consists of C104, L102, C105, C106,C107, L101 and C109. It has been optimized for efficiency of the power amplifier. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically less than 1.2 dB.

7.6.4 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U102 to regulate the power output of the radio. The current to the final stage of the power module is supplied through R104, which provides a voltage proportional to the current drain. This voltage is then fed back to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C126, C130 and C132) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

U103 and its associated components are part of the temperature cut back circuitry. It senses the printed circuit board temperature around the transmitter circuits and provides a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

7.7 800 MHz Receiver

The receiver functions are shown in Figure 7-6 and are described in the paragraphs that follow.

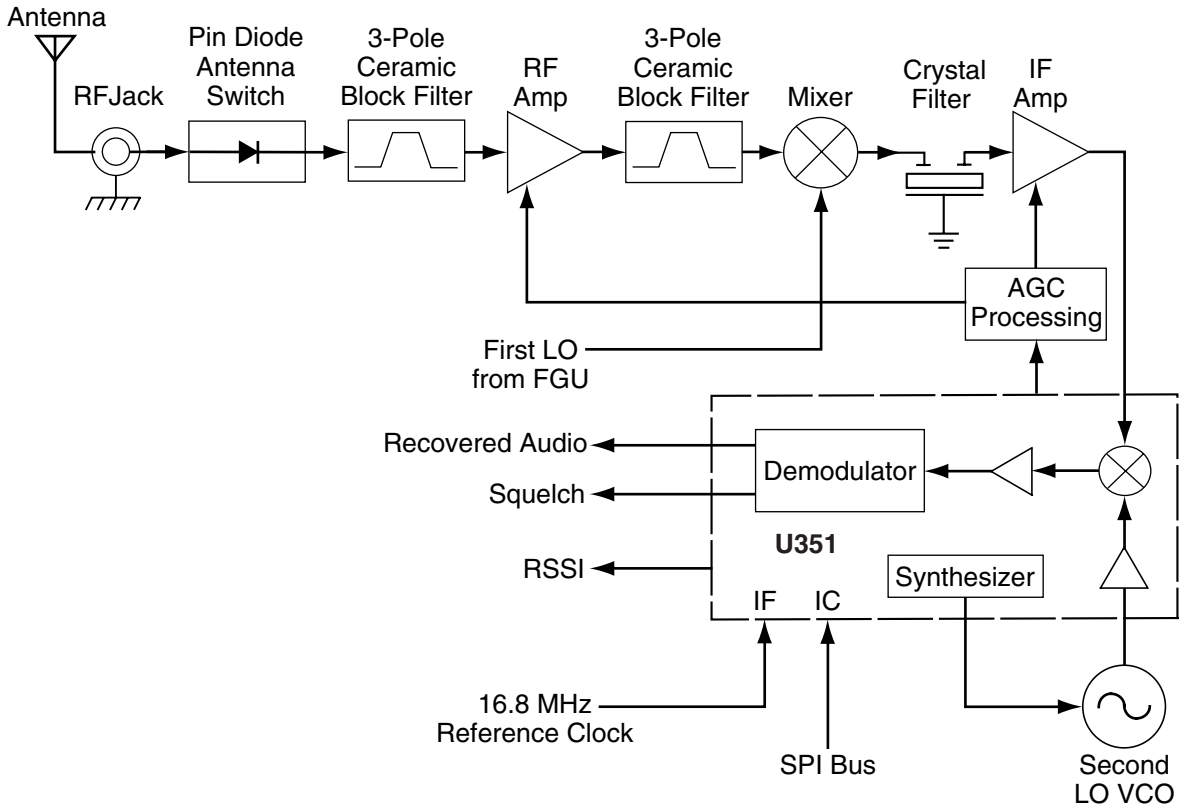


Figure 7-6. 800 MHz Receiver Block Diagram

7.7.1 Receiver Front-End

The RF signal is received by the antenna and applied to a low-pass filter. For 800 MHz, the filter consists of L101, L102, C104, C105, C106, C107, C109. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes (CR101 and CR102) and a pi network (C109, L103 and C110).The signal is then applied to a fixed tuned ceramic bandpass filter, FL300.

The output of the bandpass filter is coupled to the RF amplifier transistor Q302 via C300. The RF amplifier provides a gain of approximately 12 dB. After being amplified by the RF amplifier, the RF signal is further filtered by a second fixed tuned ceramic bandpass filter, FL301.

Both the pre and post-RF amplifier ceramic filters have similar responses. The insertion loss of each filter across the 851-870 MHz band is typically 1.8 dB.

The output of the post-RF amplifier filter is connected to the passive double balanced mixer, U301. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to the 109.65 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL350) through a resistive pad and a diplexer (C312 and L306). Matching to the input of the crystal filter is provided by L353,L354, C377, and C378. The crystal filter provides the necessary selectivity and intermodulation protection.

7.7.2 Receiver Back-End

The output of crystal filter FL350 is matched to the input of the dual gate MOSFET IF amplifier transistor U352 by components L355, R359 and C376. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). AGC voltage is applied to the second gate of U352. The IF amplifier provides a gain of about 11 dB. The amplified IF signal is then coupled into U351(pin 3) via L352, R356 and C365 which provides the matching for the IF amplifier and U351.

The IF signal applied to pin 3 of U351 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 27 of U351. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in the IF module (U351).

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U351 so that it is very close to the first IF frequency. The IF IC (U351) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO will “search” for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q350. The VCO has a varactor diode, CR350, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of R365, C391, and C392.

The IF IC (U351) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used to control the automatic gain control (AGC) circuit in both the front-end and the IF.

The demodulated signal on pin 27 of U351 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

7.7.3 Automatic Gain Control Circuit

The automatic gain control circuit provides automatic gain reduction of both the low noise amplifier in the receiver front end and the IF amplifier in the receiver backend. This action is necessary to prevent overloading of the backend IF IC.

The IF automatic gain control circuit provides approximately 50 dB of attenuation range. The signal strength indicator (RSSI) output of the IF IC produces a voltage that is proportional to the RF level at the IF input to the IF IC. This voltage is inverted by U350, R351, R353, R352, R354 and C355 and it determines the RF level at which the backend end AGC is activated as well as the slope of the voltage at the output of U350 vs. the strength of the incoming RF at the antenna. The inverted output of U350 is applied to the second gate of the IF amplifier U352 via R355. As the RF signal into the IF IC increases the following occurs:

- The RSSI voltage increases,
- The output of inverter U350 decreases, and
- The voltage applied to the second gate of the FET is reduced thus reducing the gain of the IF amplifier.

The output of inverter U350 is also used to control the receiver front end AGC.

The receiver front end automatic gain control circuit provides and additional 20 dB of gain reduction. The output of the receiver backend inverter U350 is fed into the receiver front end AGC inverter U302. The components R317, R314, and C318 determine:

- The RF level at which the front end AGC is activated, and
- The slope of the voltage at the output of U302 vs. the strength of the incoming RF at the antenna.

As the RF into the antenna increases the following occurs:

- The output voltage of the receiver backend inverter U350 decreases.
- The voltage at the output of the front end inverter U302 increases.
- The result is the forward biasing of pin diode CR301.

As the diode becomes more and more forward biased the following occurs:

- C310 loads the output of the low noise amplifier Q302 thus reducing the gain of the low noise amplifier.
- R315 and R318 provide a DC path for CR301 and also limit the current through CR301.

The blocking capacitor C317 prevents DC from the AGC stage from appearing at the input of the filter FL301.

7.7.4 Frequency Generation Circuit

The frequency generation circuit is shown in Figure 7-7. The circuit is composed of the two main ICs:

- Low Voltage Fractional-N Synthesizer, U201
- VCO/Buffer IC, U250

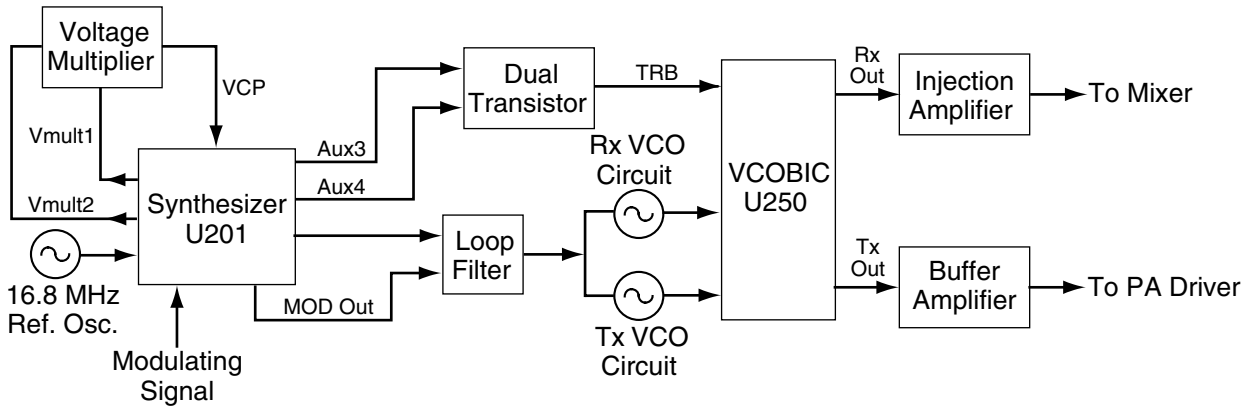


Figure 7-7. 800 MHz Frequency Generation Unit Block Diagram

Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5 V and 3.3 V which come from U247 and U248 respectively. The synthesizer in turn generates a superfiltered 4.5 V which powers U250.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3 V dc signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U201. Internally the audio is digitized by the Low Voltage Fractional-N synthesizer and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

7.8 Synthesizer

The Low Voltage Fractional-N (LV FracN) synthesizer (U201) shown in Figure 7-8 on page 7-12 uses a 16.8 MHz crystal (FL201) to provide a reference for the system. The LV FracN IC further divides this to 2.1 MHz, 2.225 MHz, and 2.4 MHz as reference frequencies. Together with C235, C236, C237, R211 and CR203, they comprise the reference oscillator which is capable of 2.5ppm stability over temperatures of -30° to 85°C. It also provides 16.8 MHz at pin 19 of U201 to be used by ASFIC and LVZIF.

Some models are equipped with a packaged 1.5ppm reference oscillator, Y200. On these models components C235, C236, C237, CR203, FL201, and R211 are not placed. Components C238, C239, C241, R212, R213, R214 and Y200 are placed instead.

The loop filter which consists of C220, C225, C226, R204, R209 and R210 provides the necessary dc steering voltage for the VCO and provides filtering of noise and spurs from U201.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put the synthesizer within the lock range. The required frequency is then locked by the normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive multiplier which is made up of D201, D202, C244, C245, C246, C247, R200, R218, C208, C243, R219, and R220. Two 3.3 V square waves (180 degrees out of phase) are applied to R219 and R220. These square waves switch alternate sets of diodes from D201 and D202, which in turn charge C244, C245, C246, and C247 in a bucket brigade fashion. The resulting output voltage that is applied to pin 47 of U201 is typically 12.8 V and allows the steering line voltage (VCO control voltage) to reach 11 V.

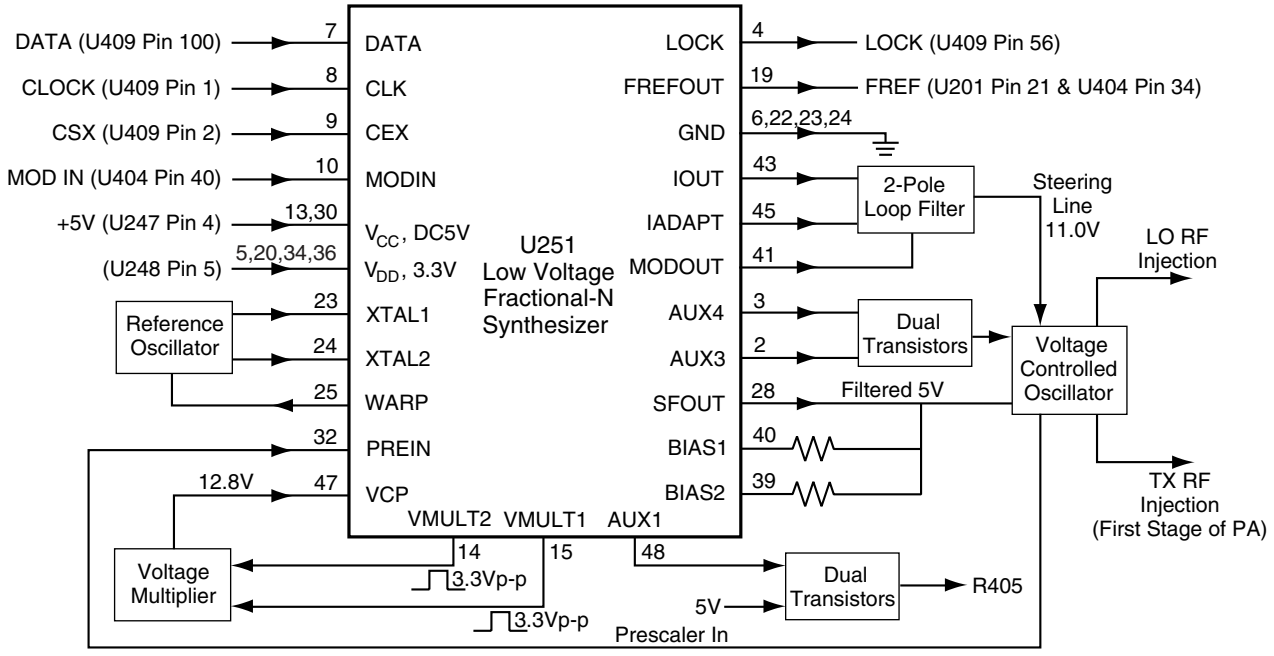


Figure 7-8. 800 MHz Synthesizer Block Diagram

7.8.1 Voltage Control Oscillator (VCO)

The voltage controlled oscillator block diagram is shown in Figure 7-9.

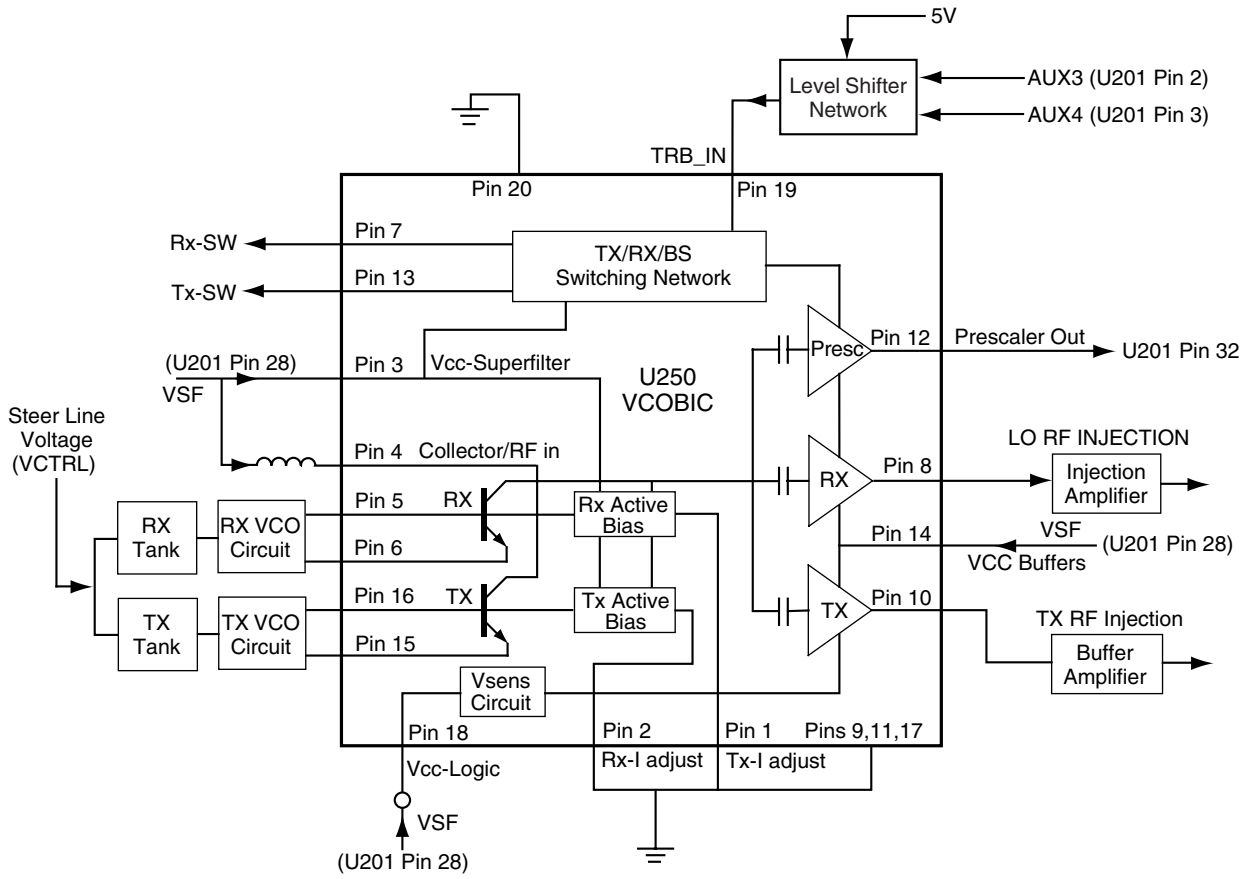


Figure 7-9. 800 MHz VCO Block Diagram

The VCOBIC (U250) in conjunction with the Low Voltage Fractional-N (LV FracN) synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U250 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U250 pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage between 2.0 V (low frequency) and 11.0 V (high frequency) when the PLL is locked on frequency.

The VCOBIC (U250) is operated at 4.54 V (VSF) and LV FracN synthesizer (U201) at 3.3 V. This difference in operating voltage requires a level shifter consisting of Q200 and Q252 on the TRB line.

The operation logic is shown in Table 7-1.

Table 7-1. Level Shifter Logic

Desired Mode	AUX 4	AUX 3	TRB
Tx	Low	High (@3.2V)	High (@4.8V)
Rx	High	Low	Low
Battery Saver	Low	Low	Hi-Z/Float (@2.5V)

In the receive mode, U250 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U250. The RF signal at U250 pin 8 is run through an injection amplifier, Q304. The resulting RF signal is the LO RF INJECTION and it is applied to the mixer at U301 (refer to *800 MHz Receiver Front End Schematic Diagram* on page 9-364).

During the transmit condition, when PTT is depressed, five volts is applied to U250 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U250. The RF signal at U250 pin 10 is amplified by Q251 and injected into the input of the PA module (U101 pin1). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through the U201 pin 41.

When a high impedance is applied to U250 pin19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

7.9 Trunked Radio Systems

Trunked systems allow a large number of users to share a relatively small number of frequencies or repeaters without interfering with each other. The airtime of all the repeaters in a trunked system is pooled, which maximizes the amount of airtime available to any one radio and minimizes channel congestion. A benefit of trunking is that the user is not required to monitor the system before transmitting.

7.9.1 Privacy Plus Trunked Systems

Privacy Plus is a proprietary trunking protocol developed by Motorola which allows a large number of users to share small amounts of frequencies without interfering with each other. The Privacy Plus configuration consists of shared multiple channel repeaters. The Privacy Plus Trunked system includes a Central Controller, which directs the users to the open channels. This kind of Trunked system requires no monitoring of the channel as in conventional systems. The Central Controller places the user in a queue to wait for a free channel. The Central Controller does the monitoring and channels selection for the user.

7.9.2 LTR™ Trunked Systems

LTR is a transmission based trunking protocol developed by the E. F. Johnson Company for primarily single site trunking applications. In transmission trunking, a repeater is used for only the duration of a single transmission. Once a transmission is completed, that repeater becomes available to other users.

7.9.3 MPT Trunked Systems

MPT (Ministry of Post and Telecommunications) developed a signalling standard (MPT1327) for trunked private land mobile radio systems. This standard defines the protocol rules for communication between a trunking system controller (TSC) and user’s radio units. The protocol offers a broad range of options which can be implemented in subsets according to user requirements. Also, there is scope for customization for special requirements, and provision made to further standardized features to be added to the protocol in the future. The standard defines only the over-air signalling and imposes only minimum constraints on system design.

7.9.4 PassPort™ Trunked Systems

PassPort is an enhanced trunking protocol developed by Trident Microsystems that supports wide area dispatch networking. A network is formed by linking several trunked sites together to form a single system. This offers users an extended communication coverage area. Additionally, users with PassPort can seamlessly roam among all sites within the network. Seamless roaming means that the radio user does not have to manually change the position on the radio when roaming from site-to-site.

For models which feature PassPort Trunking operation, the standard keypad board is replaced with the PassPort Trunking Controller Board (PTCB). This board also provides advanced voice storage features. Refer to the *PassPort Controller Schematic Diagram* on page 9-374 for connector and signal routing from, to and through the Radio, PTCB and Liquid Crystal Display (LCD) sub-systems.

7.9.4.1 Power Supplies

The radio supplies regulated Vdd of 3.3 Vdc. This is used to power the Low Speed Data Filter and Voice Storage circuits. The radio also supplies Switched Battery Voltage (SWB+). U612 regulates the SWB+ to 3.3 V which is applied to the PTCB microcontroller U601. A filtered voltage (Vdda) of _ Vdd is developed by U603-4 and is used to supply a clean reference bias for the Low Speed Data filter and Voice Storage circuits. The circuit of Q607 which can limit the voltage applied to the Voice Storage chip is not used in portable applications and is disabled by 0 Ohm resistor R614.

7.9.4.2 Microcontroller (MCU)

PassPort Trunking operation is managed by the reprogrammable FLASH ROM based microcontroller (U601). The MCU clock oscillator uses 8 MHz crystal Y601 as a stable resonator. The PTCB communicates with the main radio microcontroller by attaching to the same Serial Peripheral (SPI) bus that passes though the PTCB to the LCD on the CLK, DATA, RDY, and MISO lines. The OPT_EN line is strobed low only for communications with U601.

The MCU includes an on-chip Analog to Digital Converter (ADC). The received and filtered sub-audible low speed trunking data waveform is applied to one of the ADC inputs. The software in the MCU decodes and acts upon the trunking data.

The MCU includes a Digital to Analog Converter (DAC). As required, the MCU software generates appropriate PassPort Low Speed Trunking Data waveforms. These are applied to the Low Speed Data Filter and then to the radio transmitter modulation point. The amplitude of this waveform and the resulting transmitted deviation is controlled by software.

7.9.4.3 Low Speed Data Filter

This analog circuitry is a 4 pole, 150 Hz cutoff low pass filter comprised of U603-1, U603-2 and associated passive components. In receive mode, it removes noise and voice band signals leaving only the low speed data waveform which is applied to the ADC input of the MCU. U608-4 isolates the receive signal from the filter in transmit mode. When the radio is transmitting PassPort data, the MCU DAC low speed data waveform is applied to the input of the filter which removes harmonics that would interfere with voice and applies the resulting sub-audible data to the radio transmitter modulation point.

7.9.4.4 Keyboard Circuit

The keyboard consists of a matrix of key switches and resistors as described in Chapter 3. U605-2 monitors the column voltage and applies an interrupt signal to the radio microcontroller when any key is pressed.

7.9.4.5 BackLight Driver and LED's

The logic level signal from the radio microcontroller is translated via Q611 and applied to Q610 which uses Switched Battery Voltage (SWB+) to operate the keypad backlight LED's.

7.9.4.6 Voice Storage

The Voice Storage (VS) can be used to store audio signals coming from the receiver or from the microphone. Any stored audio signal can be played back over the radio's speaker or sent out via the radio's transmitter.

The PTCB hosts the Voice Storage circuitry. Voice Storage IC U611 provides all the required functionality and is powered from the regulated 5 volts. The mP controls U611 via SPI bus lines CLK (U611-8), DATA (U611-10) and MISO (U611-11). To transfer data, the mP first selects the U611 via line VS CS and U611 pin 9. Then the mP sends data through line DATA and receives data through line MISO. Pin 2 (RAC) of U611 indicates the end of a message row by a low state for 12.5 ms and connects to mP pin 65. A low at pin 5 (INT), which is connected to mP pin 55, indicates that the Voice Storage IC requires service from the mP.

Audio, either from the radio's receiver or from one of the microphone inputs, emerges from the ASFIC CMP (U404) at pin 43, through switch U608-1 that is selected by the mP via ASFIC CMP pin 5 (DACR) and then enters the voice storage IC U611 at pin 25. During playback, the stored audio emerges from U611 at pin 20. To transmit the audio signal, it is fed through resistive divider R657 / R658, through switch U608-3 and through line EXT MIC. When this path is selected, the audio signal enters the ASFIC CMP at pin 48 and is processed like normal transmit audio. To play the stored audio over the radio's speaker, the audio from U611 pin 20 is buffered by op-amp U605-1, through switch U608-2 and fed via line FLAT RX SND to ASFIC CMP pin 10 (UIO). In this case, this ASFIC CMP pin is programmed as input and feeds the audio signal through the normal receiver audio path to the speaker or handset. Switches U608-2 and U608-3 are controlled by the mP via ASFIC CMP pin 6 (DACG) and feed the stored audio only to the ASFIC CMP port UIO when it is programmed as input.

7.10 900 MHz Transmitter

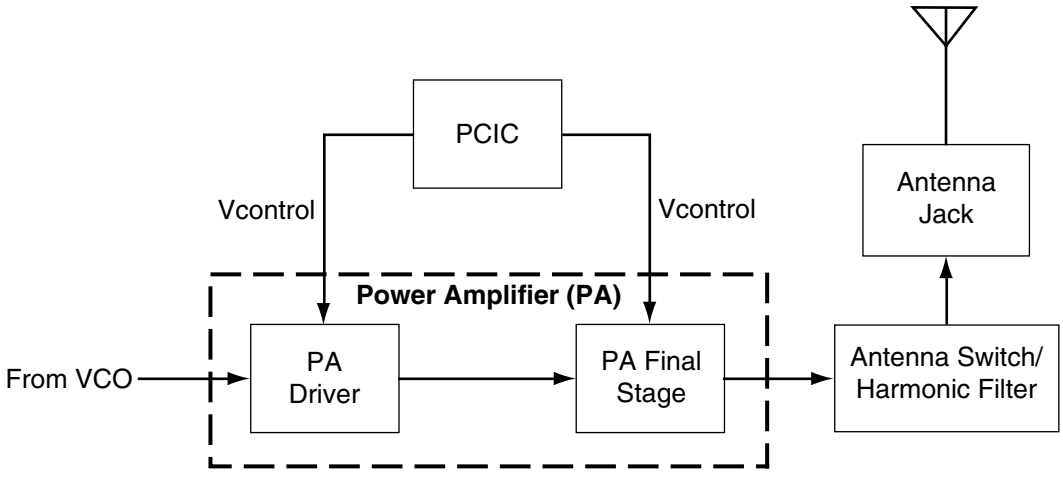


Figure 7-10. Transmitter Block Diagram

The 900 MHz transmitter shown in Figure 7-10 on page 7-16 contains the following basic circuits:

- Power amplifier
- Antenna switch
- Harmonic filter
- Power control integrated circuit (PCIC).

7.10.1 Power Amplifier

The power amplifier consists of two devices:

- 5185130C65 driver IC (U101) and
- 4813828A09 LDMOS PA (Q101).

The 30C65 driver IC contains a 2 stage amplification with a supply voltage of 7.5 V.

This RF driver IC is capable of supplying an output power of 0.3W (pin 6 and 7) with an input signal of 2.5mW (4dBm) (pin16). The current drain would typically be 200mA while operating in the frequency range of 896-941 MHz.

The 28A09 LDMOS PA is capable of supplying an output power of 4.5 W with an input signal of 0.3 W. The current drain would typically be 1100mA while operating in the frequency range of 896-941 MHz. The power out can be varied by changing the biasing voltage and the drive level from the driver IC.

7.10.2 Antenna Switch

The antenna switch circuit consists of two PIN diodes (CR101 and CR102), a pi network (C115, L109 and C138), and three current limiting resistors (R102, R103, R106). In the transmit mode, B+ at PCIC (U102) pin32 will go high, applying a B+ bias to the antenna switch circuit to bias the diodes “on”. The shunt diode (CR102) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

7.10.3 Harmonic Filter

The harmonic filter consists of L104, L105, C114, C115, C124,C125, and C126. It has been optimized for efficiency of the power amplifier. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically 0.9 dB, and less than 1.2 dB.

7.10.4 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U102 to regulate the power output of the radio. The current to the final stage of the power module is supplied through R101, which provides a voltage proportional to the current drain. This voltage is then fed back to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C156, C157, and C158) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

U103 and its associated components are part of the temperature cut back circuitry. It senses the printed circuit board temperature around the transmitter circuits and output a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

7.11 900 MHz Receiver

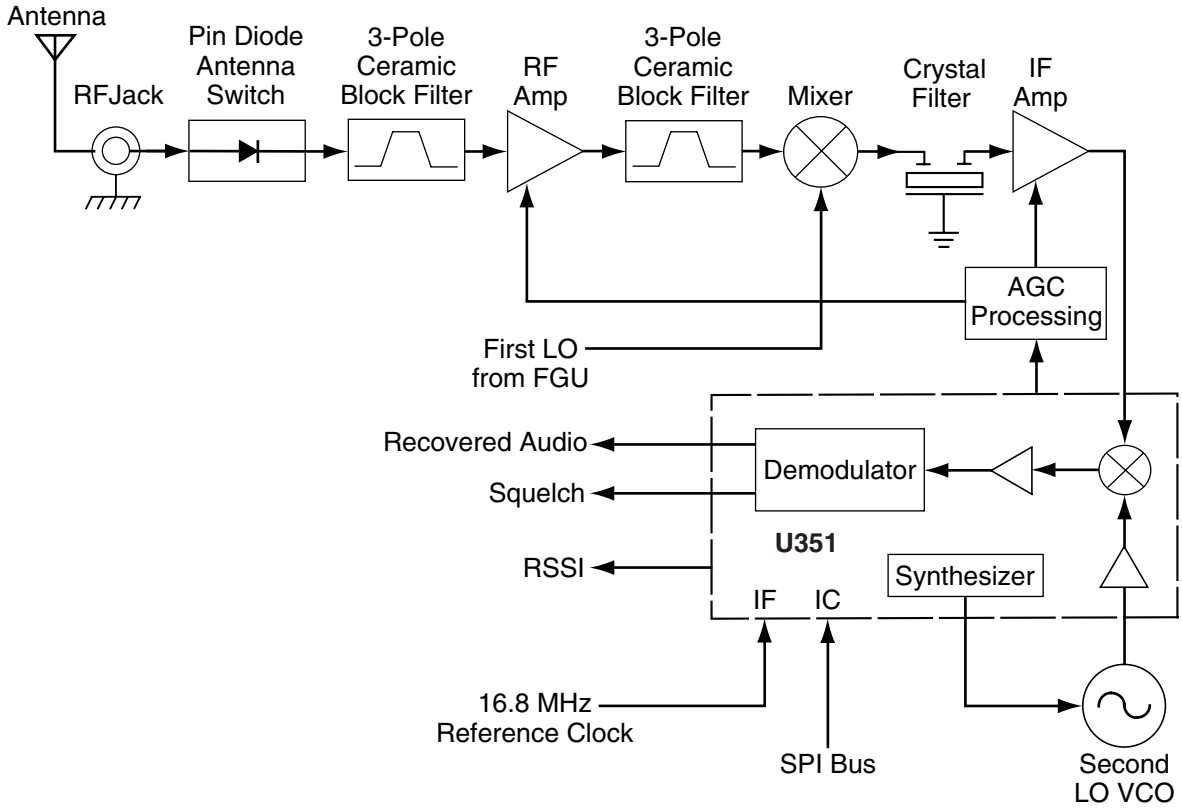


Figure 7-11. 900 MHz Receiver Block Diagram

7.11.1 Receiver Front-End

The RF signal is received by the antenna and applied to a low-pass filter. For 900 MHz, the filter consists of L104, L105, C114, C115, C124, C125, and C126. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes(CR101, and CR102) and a pi network (C115, L109, and C138). The signal is then applied to a fixed tuned ceramic bandpass filter, FL300.

The output of the bandpass filter is coupled to the RF amplifier transistor Q302 via C300. The RF amplifier provides a gain of approximately 14 dB. After being amplified by the RF amplifier, the RF signal is further filtered by a second fixed tuned ceramic bandpass filter, FL301.

Both the pre and post-RF amplifier ceramic filters have similar responses. The insertion loss of each filter across the 935-941 MHz band is less than 2 dB.

The output of the post-RF amplifier filter is connected to the passive double balanced mixer, U301, through matching components C321, and L311. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to the 109.65 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL350) through a resistor pad and a diplexer (C312, and L306). Matching to the input of the crystal filter is provided by L353, L354, C377, and C378. The crystal filter provides some of the necessary selectivity, and intermodulation protection.

7.11.2 Receiver Back-End

The output of crystal filter FL350 is matched to the input of the dual gate MOSFET IF amplifier transistor U352 by components L355, R359, and C376. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). AGC voltage is applied to the second gate of U352. The IF amplifier provides a gain of about 11dB. The amplified IF signal is then coupled into U351(pin 3) via L352, R356 and C365 which provides the matching for the IF amplifier and U351.

The IF signal applied to pin 3 of U351 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 27 of U351. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in the IF module (U351).

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U351 so that it is very close to the first IF frequency. The IF IC (U351) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO will “search” for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q350. The VCO has a varactor diode, CR350, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of R365, C391, and C392.

The IF IC (U351) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used to control the automatic gain control (AGC) circuit in both the front-end and the IF.

The demodulated signal on pin 27 of U351 is also used for squelch control. The signal is routed to U851 where a “flutter fighter” process is implemented. The signal leaves U851 via pin F4 and is then routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

7.11.3 Hear Clear IC

Hear Clear (HC) IC is typically used for 900 MHz radios. The HC IC comprises three main internal circuit blocks:

- Compressor,
- Flutter Fighter
- Expander Circuits.

Only the Flutter Fighter section of this IC is used by this radio. The Compressor and the Expander are included in the ASFIC. There are six enable/control lines on the Hear Clear IC which determine the ICs mode of operation. The Flutter Fighter Enable line (U851-E3) is controlled by ASFIC DACRX line (U404-4). The logic control and the IC status is summarized in Table 7-2 on page 7-20.

Table 7-2. Hear Clear Logic and IC Status

Name	Ref. Des	Set By	RX1*	RX2**
IC Enable	U851-C4	SWB+	1	1
Flutter Fighter Enable	U851-E3	DACRX	1	0
LO Clamp Disable	U851-A5	SWB+	1	1
LO Clamp Disable	U851-C2	GND	0	0
HCI Disable	U851-B6	SWB+	1	1
LO Clamp Disable	U851-D1	GND	0	0

**RX1:receive voice with carrier squelch, PL or DPL (Flutter Fighter can be on or off).*
***RX2:refers to receive mode with all other data HST/MDC/DTMF (Flutter Fighter must be off).*

7.11.3.1 Receive Path for Radios with Hear Clear

The audio signal enters Hear Clear controller from DEMOD_OUT signal on DISC. The detected audio “DISC” enters the Hear Clear Flutter Fighter through C857 and C859. C857 connects the signal to FF IN (U851-E4). C859 is a beginning of a noise sampling circuit consisting of components – C859, R853, C860, R854, C861, R855 and C862; and Hear Clear Ports Ref, Noise Filter In, and Noise Filter Out, Noise Hold.

After exiting Hear Clear at the “FF OUT” (U851-F4), the signal enters ASFIC at DISC (U404-2). Within the ASFIC, the signal passes through a low pass filter and high pass filter limiting the audio bandwidth to 300 Hz-3 kHz. It then goes through de-emphasis and exits the ASFIC at AUDIO (U404-41). The audio is then routed to the Audio PA in the same manner as the standard receive audio.

The purpose of the Flutter Fighter is to sample the amount of Noise in the receive audio between 10-20 kHz using the Noise Filter (U851-B5), Noise Filter Out (U851-C6), and Noise Hold (U851-D5). In addition, it monitors the rate of change of RSSI (Receive Signal Strength In) (U303-1). The detected audio DISC enters into the Hear Clear IC at “FF IN” (U851-E4). The circuit then reduces the amount of popping Noise associated with fading. The improved audio exits the IC at “FF OUT” (U851-F4).

7.11.3.2 Hear Clear Routing of Data/Signaling

While receiving, sub-audible signals PL/DPL go through the Flutter Fighter along with the audio, and is unaffected by the Flutter Fighter operation. On entering the ASFIC, the sub-audible signaling is separated from the voice and decoded.

While receiving other signals HST/MDC (not sub-audible), the Flutter Fighter is set to the “pass through mode”. In this mode, the Flutter Fighter is routed from ”FF IN” to “FF OUT” without any processing.

7.11.4 Automatic Gain Control Circuit

The automatic gain control circuit provides automatic gain reduction of both the low noise amplifier in the receiver front end and the IF amplifier in the receiver backend. This action is necessary to prevent overloading of the backend IF IC.

The IF automatic gain control circuit provides approximately 50 dB of attenuation range. The signal strength indicator (RSSI) output of the IF IC produces a voltage that is proportional to the RF level at the IF input to the IF IC. This voltage is inverted by U350, R351, R353, R352, R354 and C355 and it determines the RF level at which the backend end AGC is activated as well as the slope of the voltage at the output of U350 vs. the strength of the incoming RF at the antenna. The inverted output of U350 is applied to the second gate of the IF amplifier U352 via R355. As the RF signal into the IF IC increases the following occurs:

- The RSSI voltage increases,
- The output of inverter U350 decreases, and
- The voltage applied to the second gate of the FET is reduced thus reducing the gain of the IF amplifier.

The output of inverter U350 is also used to control the receiver front end AGC.

The receiver front end automatic gain control circuit provides and additional 20 dB of gain reduction. The output of the receiver back end inverter U350 is fed into the receiver front end AGC inverter U302. The components R317, R314, and C318 determine:

- The RF level at which the front end AGC is activated, and
- The slope of the voltage at the output of U302 vs. the strength of the incoming RF at the antenna.

As the RF into the antenna increases the following occurs:

- The output voltage of the receiver back end inverter U350 decreases.
- The voltage at the output of the front end inverter U302 increases.
- The result is the forward biasing of pin diode CR301.

As the diode becomes more and more forward biased the following occurs:

- C310 loads the output of the low noise amplifier Q302 thus reducing the gain of the low noise amplifier.
- R315 and R318 provide a DC path for CR301 and also limit the current through CR301.

The blocking capacitor C317 prevents DC from the AGC stage from appearing at the input of the filter FL301.

7.12 Frequency Generation Circuitry

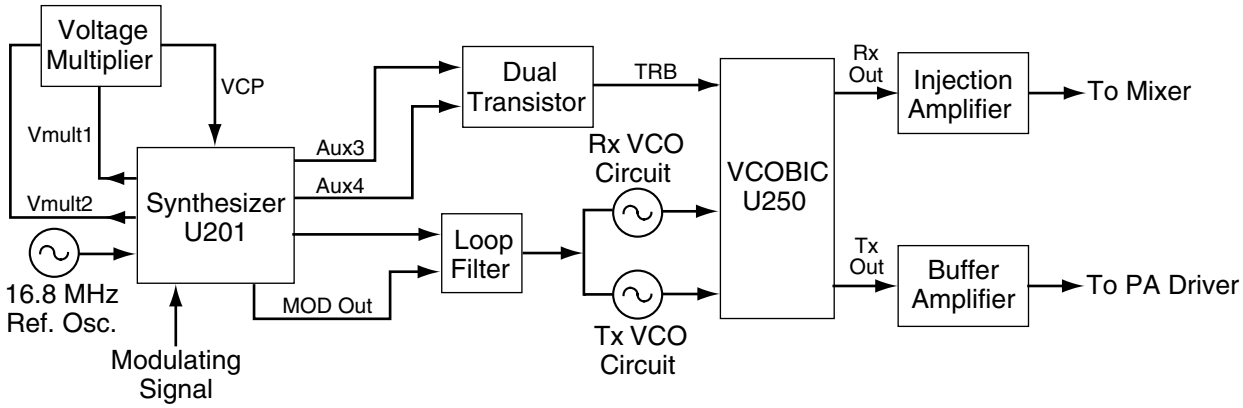


Figure 7-12. Frequency Generation Unit Block Diagram

The Frequency Generation circuitry is comprised of two main ICs, the Low Voltage Fractional-N (LV FracN) synthesizer (U201), and the VCO/Buffer IC (U250). Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5 V and 3.3 V which come from U247 and U248 respectively. The synthesizer in turn generates a superfiltered 4.5 V which powers U250.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3 V dc signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U201. Internally the audio is digitized by the LV FracN IC and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

7.13 900 MHz Synthesizer

The Low Voltage Fractional-N (LV FracN) synthesizer (U201) uses a 16.8 MHz packaged 1.5 ppm reference oscillator (Y200) to provide a reference for the system. The LV FracN IC further divides the 16.8 MHz to 2.1 MHz, 2.225 MHz, and 2.4 MHz. Y200, together with C238, C239, C241, R212, R213, and R214 comprise the reference oscillator which is capable of 1.5 ppm stability over temperatures of -30° to 85°C. It also provides 16.8 MHz at pin 19 of U201 to be used by ASFIC and LVZIF.

The loop filter which consists of C801, C802, C803, C804, C805, C225, C226, R204, R209, and R210 provides the necessary dc steering voltage for the VCO and provides filtering of noise and spurs from U201.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put the synthesizer within the lock range. The required frequency is then locked by the normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive multiplier which is made up of CR201, CR202, C244, C245, C246, C247, R200, R218, C208, C243, R219, and R220. Two 3.3 V square waves (180 degrees out of phase) are applied to R219 and R220. These square waves switch alternate sets of diodes from CR201 and CR202, which in turn charge C244, C245, C246, and C247 in a bucket brigade fashion. The resulting output voltage that is applied to pin 47 of U201 is typically 12.8 V and allows the steering line voltage (VCO control voltage) to reach 11 V.

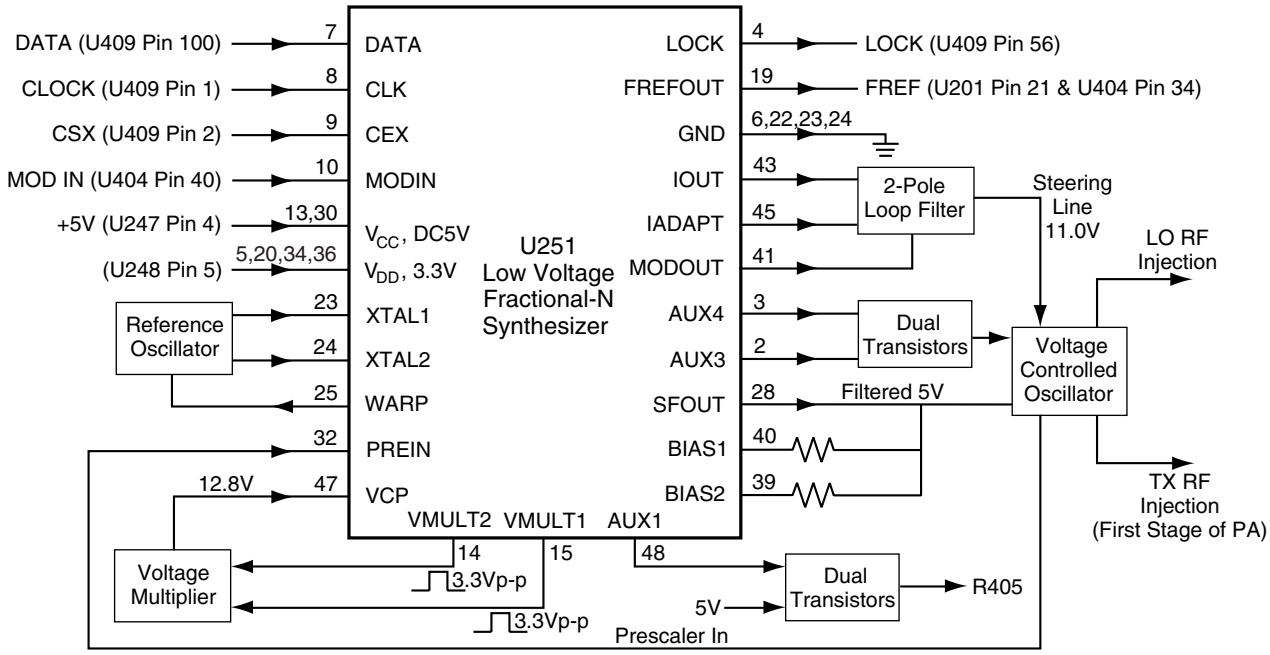


Figure 7-13. Synthesizer Block Diagram

7.14 900 MHz Voltage Control Oscillator (VCO)

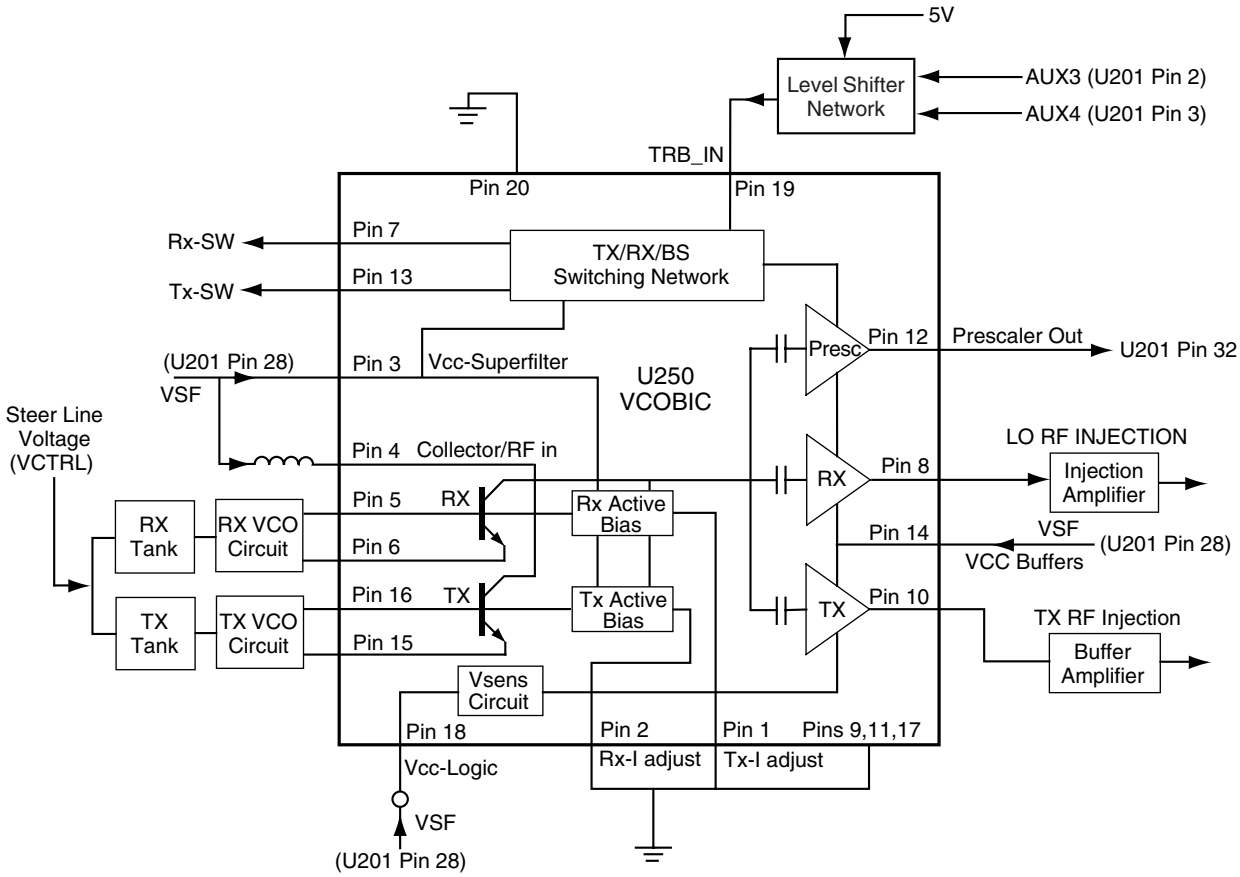


Figure 7-14. VCO Block Diagram

The VCOBIC (U250) in conjunction with the LV FracN synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U250 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U250 pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage between 2.0 V (low frequency) and 11.0 V (high frequency) when the PLL is locked on frequency.

The VCOBIC (U250) is operated at 4.54 V (VSF) and LV FracN synthesizer (U201) at 3.3 V. This difference in operating voltage requires a level shifter consisting of Q200 and Q252 on the TRB line.

The operation logic is shown in Table 7-3.

Table 7-3. Level Shifter Logic

Desired Mode	AUX 4	AUX 3	TRB
Tx	Low	High (@3.2V)	High (@4.8V)
Rx	High	Low	Low
Battery Saver	Low	Low	Hi-Z/Float (@2.5V)

In the receive mode, U250 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U250. The RF signal at U250 pin 8 is run through an injection amplifier, Q304. The resulting RF signal is the LO RF INJECTION and it is applied to the mixer at U301.

During the transmit condition, when PTT is depressed, five volts is applied to U250 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U250. The RF signal at U250 pin 10 is amplified by Q251 and injected into the input of the PA module (U101 pin1). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through the U201 pin 41.

When a high impedance is applied to U250 pin19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

Chapter 8 Maintenance

8.1 Introduction

This chapter of the manual describes:

- Preventive maintenance
- Safe handling of CMOS devices
- Repair procedures and techniques

8.2 Preventive Maintenance

The radios do not require a scheduled preventive maintenance program; however, periodic visual inspection and cleaning is recommended.

8.3 Inspection

Check that the external surfaces of the radio are clean, and that all external controls and switches are functional. It is not recommended to inspect the interior electronic circuitry.

8.3.1 Cleaning

The following procedures describe the recommended cleaning agents and the methods to be used when cleaning the external and internal surfaces of the radio. External surfaces include the front cover, housing assembly, and battery case. These surfaces should be cleaned whenever a periodic visual inspection reveals the presence of smudges, grease, and/or grime.

NOTE: Internal surfaces should be cleaned only when the radio is disassembled for servicing or repair.

The only recommended agent for cleaning the external radio surfaces is a 0.5% solution of a mild dishwashing detergent in water. The only factory recommended liquid for cleaning the printed circuit boards and their components is isopropyl alcohol (70% by volume).

CAUTION: The effects of certain chemicals and their vapors can have harmful results on certain plastics. Aerosol sprays, tuner cleaners, and other chemicals should be avoided.

1. **Cleaning External Plastic Surfaces**
   The detergent-water solution should be applied sparingly with a stiff, non-metallic, short-bristled brush to work all loose dirt away from the radio. A soft, absorbent, lintless cloth or tissue should be used to remove the solution and dry the radio. Make sure that no water remains entrapped near the connectors, cracks, or crevices.
2. **Cleaning Internal Circuit Boards and Components**
   Isopropyl alcohol may be applied with a stiff, non-metallic, short-bristled brush to dislodge embedded or caked materials located in hard-to-reach areas. The brush stroke should direct the dislodged material out and away from the inside of the radio. Make sure that controls or tunable components are not soaked with alcohol. Do not use high-pressure air to hasten the drying process since this could cause the liquid to collect in unwanted places. Upon completion of the cleaning process, use a soft, absorbent, lintless cloth to dry the area. Do not brush or apply any isopropyl alcohol to the frame, front cover, or back cover.

NOTE: Always use a fresh supply of alcohol and a clean container to prevent contamination by dissolved material (from previous usage).

8.4 Safe Handling of CMOS and LDMOS

Complementary metal-oxide semiconductor (CMOS) and lateral diffusion metal oxide semiconductor (LDMOS) devices are used in this family of radios. Their characteristics make them susceptible to damage by electrostatic or high voltage charges. Damage can be latent, resulting in failures occurring weeks or months later. Therefore, special precautions must be taken to prevent device damage during disassembly, troubleshooting, and repair.

Handling precautions are mandatory for the circuits and are especially important in low humidity conditions. DO NOT attempt to disassemble the radio without first referring to the CMOS CAUTION paragraph in the Disassembly and Reassembly section of the basic manual.

8.5 General Repair Procedures and Techniques

- **Parts Replacement and Substitution**
  When damaged parts are replaced, identical parts should be used. If the identical replacement component is not locally available, check the parts list for the proper Motorola part number and order the component from the nearest Motorola Communications parts center listed in the “Piece Parts” section of this manual (See Chapter 1).
- **Rigid Circuit Boards**
  The family of radios uses bonded, multi-layer, printed circuit boards. Since the inner layers are not accessible, some special considerations are required when soldering and unsoldering components. The printed-through holes may interconnect multiple layers of the printed circuit. Therefore, care should be exercised to avoid pulling the plated circuit out of the hole.

  When soldering near the 20-pin and 40-pin connectors:
  - Avoid accidentally getting solder in the connector.
  - Be careful not to form solder bridges between the connector pins.
  - Closely examine your work for shorts due to solder bridges.

- **Flexible Circuits**
  The flexible circuits are made from a different material than the rigid boards and different techniques must be used when soldering. Excessive prolonged heat on the flexible circuit can damage the material. Avoid excessive heat and excessive bending.

  For parts replacement, use the ST-1087 Temperature-Controlled Solder Station with a 600-700 degree tip, and use small diameter solder such as ST-633. The smaller size solder will melt faster and require less heat to be applied to the circuit.

  To replace a component on a flexible circuit:
  1. Grasp the edge of the flexible circuit with seizers (hemostats) near the part to be removed.
  2. Pull gently.
  3. Apply the tip of the soldering iron to the component connections while pulling with the seizers.

  Do not attempt to puddle out components. Prolonged application of heat may damage the flexible circuit.

- **Chip Components**
  Use either the RLN-4062 Hot-Air Repair Station or the Motorola 0180381B45 Repair Station for chip component replacement. When using the 0180381B45 Repair Station, select the TJ-65 mini-thermojet hand piece. On either unit, adjust the temperature control to 700 degrees F. (370 degrees C), and adjust the airflow to a minimum setting. Airflow can vary due to component density.

  To remove a chip component:

  1. Use a hot-air hand piece and position the nozzle of the hand piece approximately 1/8” (0.3 cm) above the component to be removed.
  2. Begin applying the hot air. Once the solder reflows, remove the component using a pair of tweezers.
  3. Using a solder wick and a soldering iron or a power desoldering station, remove the excess solder from the pads.

  To replace a chip component using a soldering iron:

  1. Select the appropriate micro-tipped soldering iron and apply fresh solder to one of the solder pads.
  2. Using a pair of tweezers, position the new chip component in place while heating the fresh solder.
  3. Once solder wicks onto the new component, remove the heat from the solder.
  4. Heat the remaining pad with the soldering iron and apply solder until it wicks to the component. If necessary, touch up the first side. All solder joints should be smooth and shiny.

  To replace a chip component using hot air:

  1. Use the hot-air hand piece and reflow the solder on the solder pads to smooth it.
  2. Apply a drop of solder paste flux to each pad.
  3. Using a pair of tweezers, position the new component in place.
  4. Position the hot-air hand piece approximately 1/8” (0.3 cm) above the component and begin applying heat.
  5. Once the solder wicks to the component, remove the heat and inspect the repair. All joints should be smooth and shiny.

- **Shields**
  Removing and replacing shields will be done with the R-1070 station with the temperature control set to approximately 415°F (215°C) [445°F (230°C) maximum].

  To remove the shield:

  1. Place the circuit board in the R-1070’s holder.
  2. Select the proper heat focus head and attach it to the heater chimney.
  3. Add solder paste flux around the base of the shield.
  4. Position the shield under the heat-focus head.
  5. Lower the vacuum tip and attach it to the shield by turning on the vacuum pump.
  6. Lower the focus head until it is approximately 1/8” (0.3 cm) above the shield.
  7. Turn on the heater and wait until the shield lifts off the circuit board.
  8. Once the shield is off, turn off the heat, grab the part with a pair of tweezers, and turn off the vacuum pump.
  9. Remove the circuit board from the R-1070’s circuit board holder.

To replace the shield:

1. Add solder to the shield if necessary, using a micro-tipped soldering iron.
2. Next, rub the soldering iron tip along the edge of the shield to smooth out any excess solder. Use solder wick and a soldering iron to remove excess solder from the solder pads on the circuit board.
3. Place the circuit board back in the R1070's circuit board holder.
4. Place the shield on the circuit board using a pair of tweezers.
5. Position the heat-focus head over the shield and lower it to approximately 1/8" (0.3 cm) above the shield.
6. Turn on the heater and wait for the solder to reflow.
7. Once complete, turn off the heat, raise the heat-focus head and wait approximately one minute for the part to cool.
8. Remove the circuit board and inspect the repair. No cleaning should be necessary.

8.6 Recommended Test Tools

Table 8-1 lists the recommended tools used for maintaining this family of radios. These tools are also available from Motorola.

Table 8-1. Recommended Test Tools

Motorola Part Number	Description	Application
RSX4043	Torx Driver	Tighten and remove chassis screws.
6680387A70	T-6 Torx Bit	Removable Torx driver bit.
R1453A	Digital readout solder station	Digitally controlled soldering iron.
0180386A78	Illuminated magnifying glass with lens attachment.	
0180386A82 6684253C72 6680384A98 1010041A86 1080303E45	Anti-static grounding kit Straight prober Brush Solder (RMA type), 63/37, 0.5mm diameter 1 lb. spool SMD tool kit (included with R1319A)	Used during all radio assembly and disassembly procedures.
R1319A (110V) or R1321A(220V)	ChipMaster Surface Mount Rework Station	Removal and assembly of surface-mounted integrated circuits and shields includes 5 nozzles.
R1364A	Digital Heated Tweezer System	Chip component removal.
R1427A	Board Preheater	Reduces heatsink on multi level boards.
8880309B53	Rework Equipment Catalog	Contains application notes, procedures and technical rework equipment.

8.7 Replacing the Circuit Board Fuse

In cases where the radio fails to turn on when power is applied, the circuit board fuse should always be checked as a probable cause of the failure. The locations of the fuse for both the UHF and VHF boards are shown in Figure 8-1 on page 8-6. The radio must be disassembled to replace the fuses as described in the Basic Service Manual (see section 1.3 on page 1-2), then the circuit board separated from the radio chassis as described in the paragraphs that follow.

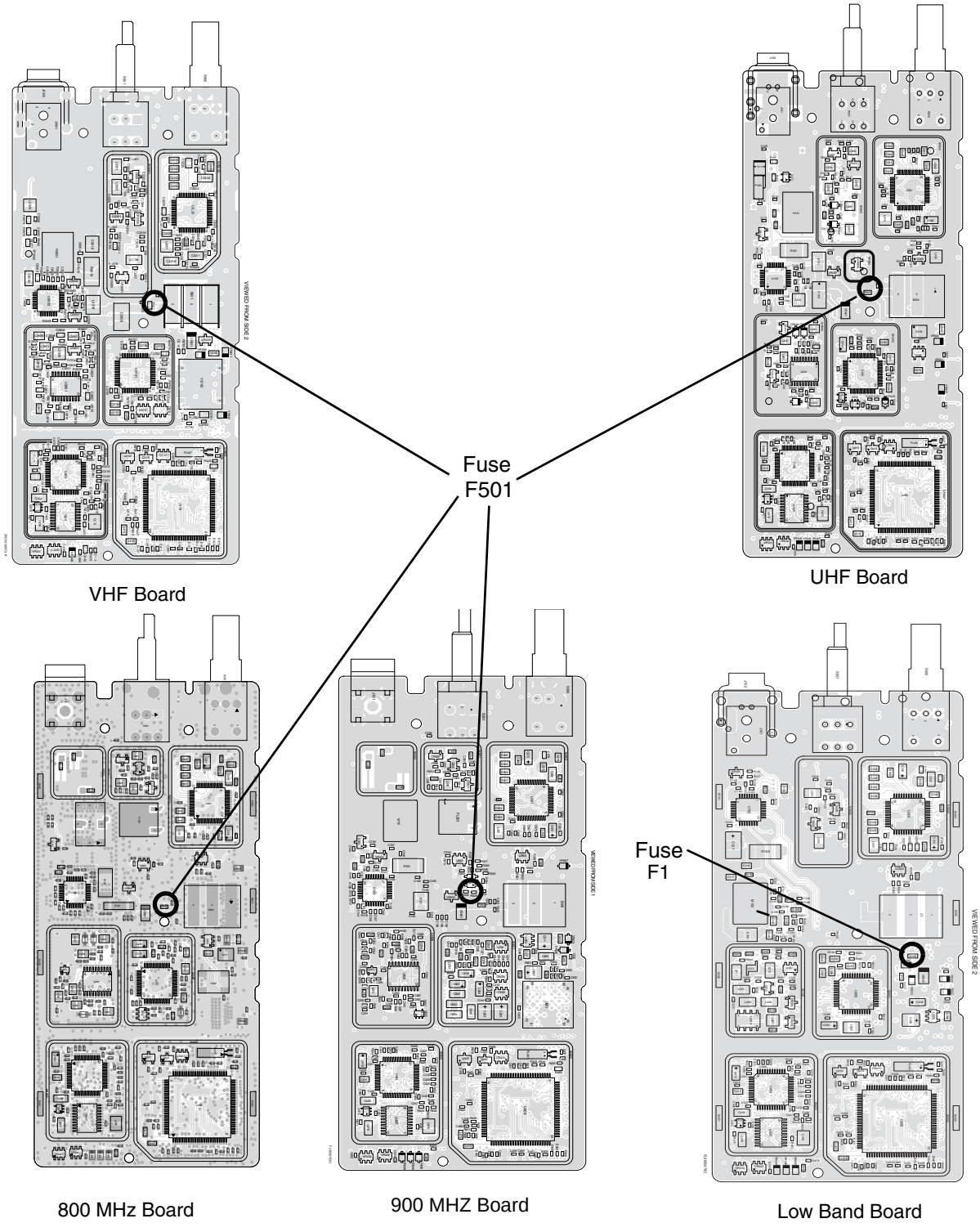


Figure 8-1. UHF/VHF/Low Band/800 MHz/900 MHz Circuit Board Fuse Locations

8.8 Removing and Reinstalling the Circuit Board

Both the UHF and VHF circuit boards are removed from the radio chassis in the following manner:

1. Refer to the Basic Service Manual (see Table 1-1, “Related Documents,” on page 1-2) for radio disassembly, then use a Torx driver and a T-6 bit to remove the four Torx screws shown in Figure 8-2.
2. Lift the circuit board out of the radio chassis, then remove and discard the thermal pad located between the circuit board and chassis.
3. After repairs, replace the thermal pad (Motorola P/N 7580556Z01) then reinstall the circuit board into the radio chassis.
4. Reinstall and tighten the four Torx screws to secure the circuit board to the chassis.
5. Refer to the Basic Service Manual to reassemble the radio.

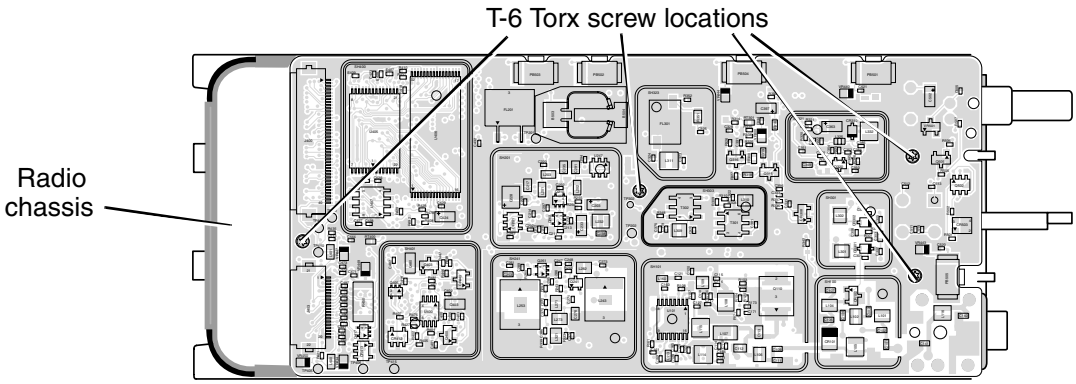


Figure 8-2. Circuit Board Removal and Reinstallation

8.9 Power Up Self-Test Error Codes

Turning on the radio starts a self-test routine that checks the RAM, ROM checksum, EEPROM hardware and EEPROM checksum. If these checks are successful, the radio generates two high-pitched self-test pass tones. If the self-test is not successful, one low-pitched tone is heard. Radios with displays are able to display the error codes. The displayed error codes and related corrections are as follows:

Table 8-2. Power Up Self-Test Error Codes

If the error code displayed is ...	Then, there is a ...	To correct the problem ...
“RAM TST ERROR”	RAM test failure.	retest the radio by turning it off and turning it on again. If message reoccurs, replace RAM (U405).
“ROM CS ERROR”	wrong ROM checksum.	replace ROM (U406).
“EEPRM HW ERROR”	codeplug structure mismatch or non existence of codeplug.	reprogram codeplug with correct version and retest radio. If message reoccurs, replace EEPROM (U407).
“EEPRM CS ERROR”	wrong codeplug checksum.	reprogram codeplug.

Table 8-2. Power Up Self-Test Error Codes (Continued)

If the error code displayed is ...	Then, there is a ...	To correct the problem ...
No Display	improperly connected display module or damaged display module.	check connection between main board and display module or replace with new display module.

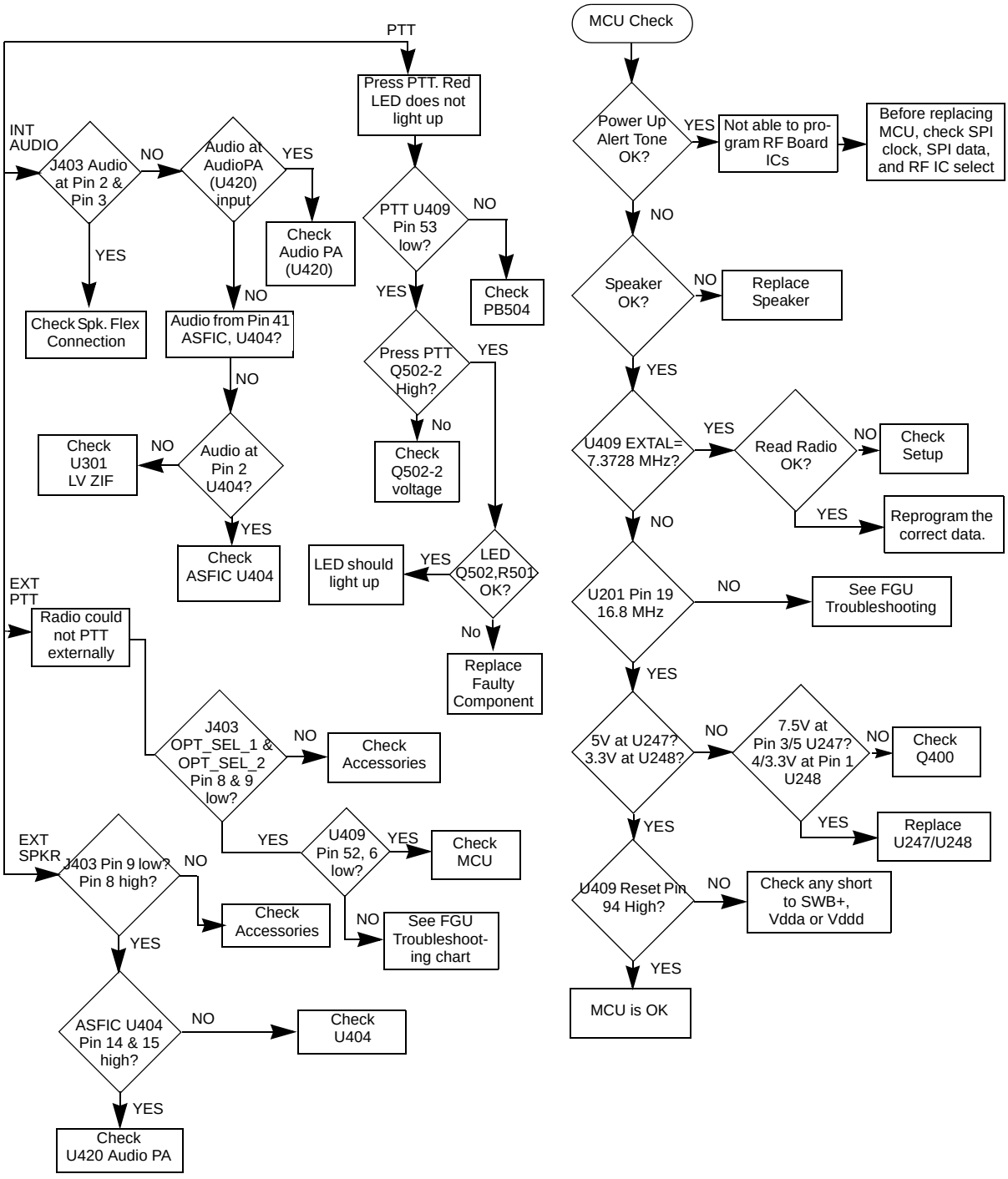
For LTR Models:

Table 8-3. Power Up Self-Test Error Codes (LTR Models)

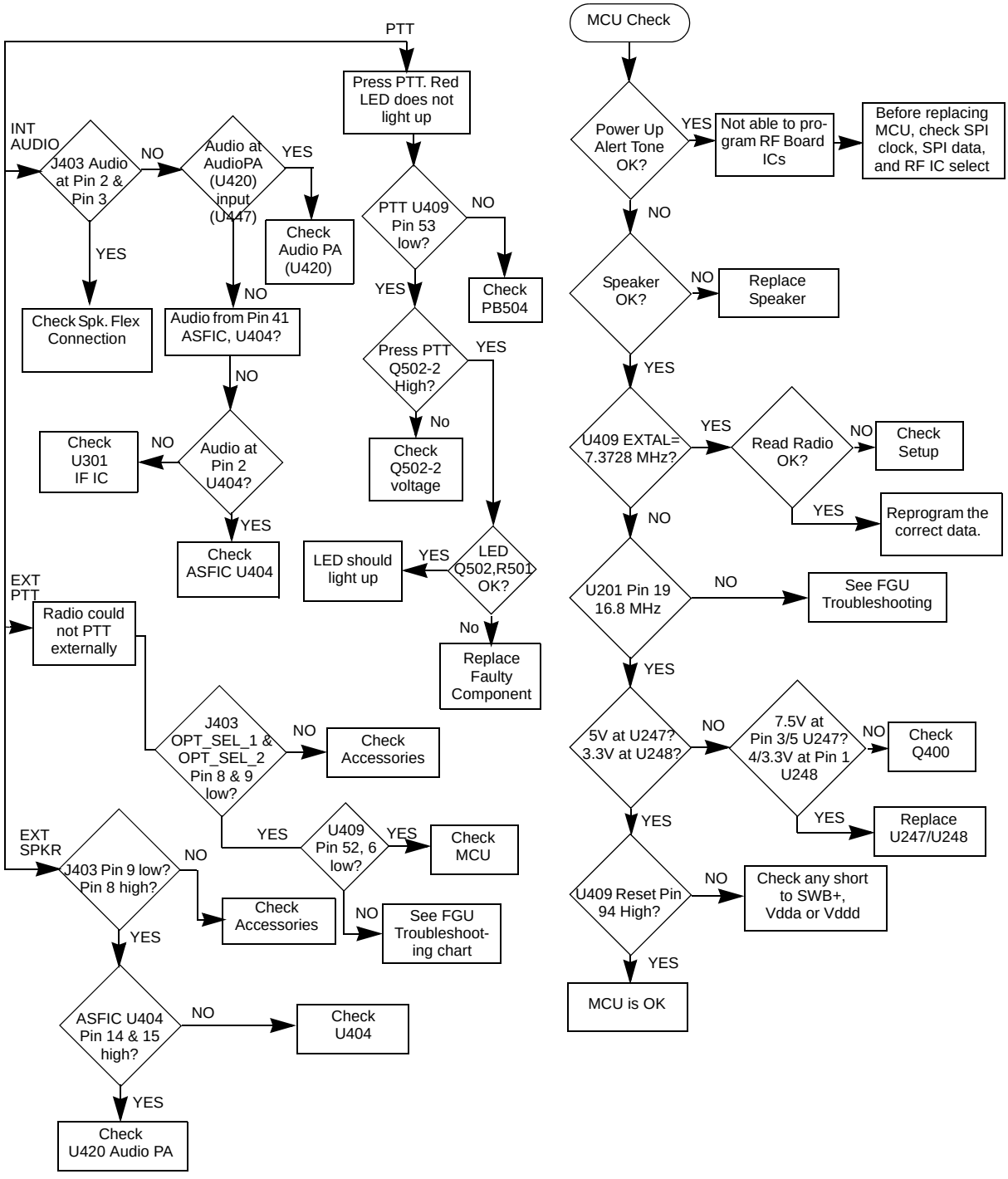
If the error code displayed is ...	Then, there is a ...	To correct the problem ...
ESN BAD	defective PTCB	return to factory for PTCB replacement.
AppCode Fail	defective PTCB firmware	reflash PTCB firmware.
EER: Watchdog	firmware failure	restart radio
Unprogrammed	programming error	use CPS to properly program radio and PTCB.
ERROR: NO PTG	no primary talk group	use CPS to program zone with a Primary Talk Group.
Backdoor	---	turn radio off and restart.

8.10 UHF Band 1 Troubleshooting Charts

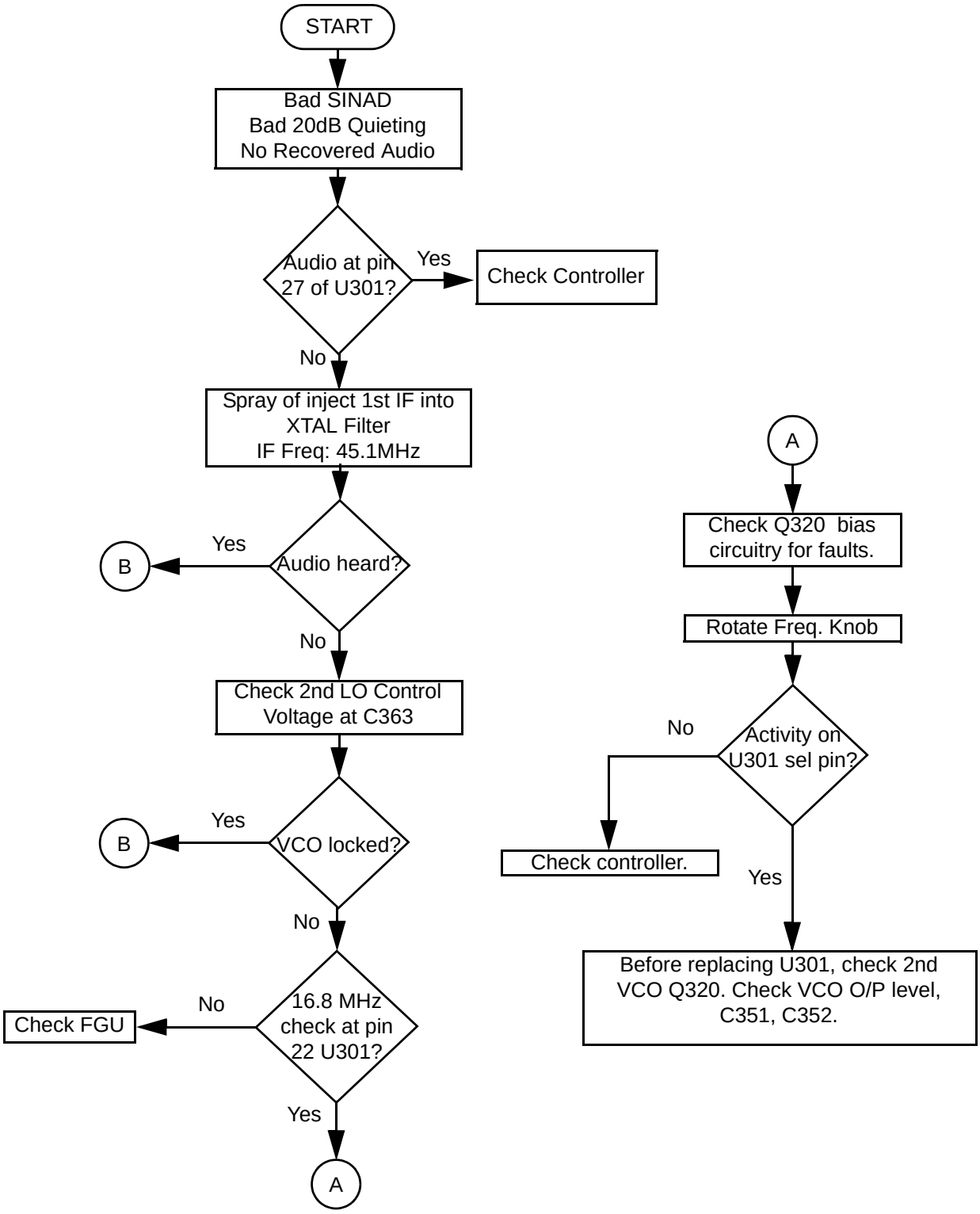
8.10.1 Troubleshooting Flow Chart for Controller for all models except PCB 8486458Z03



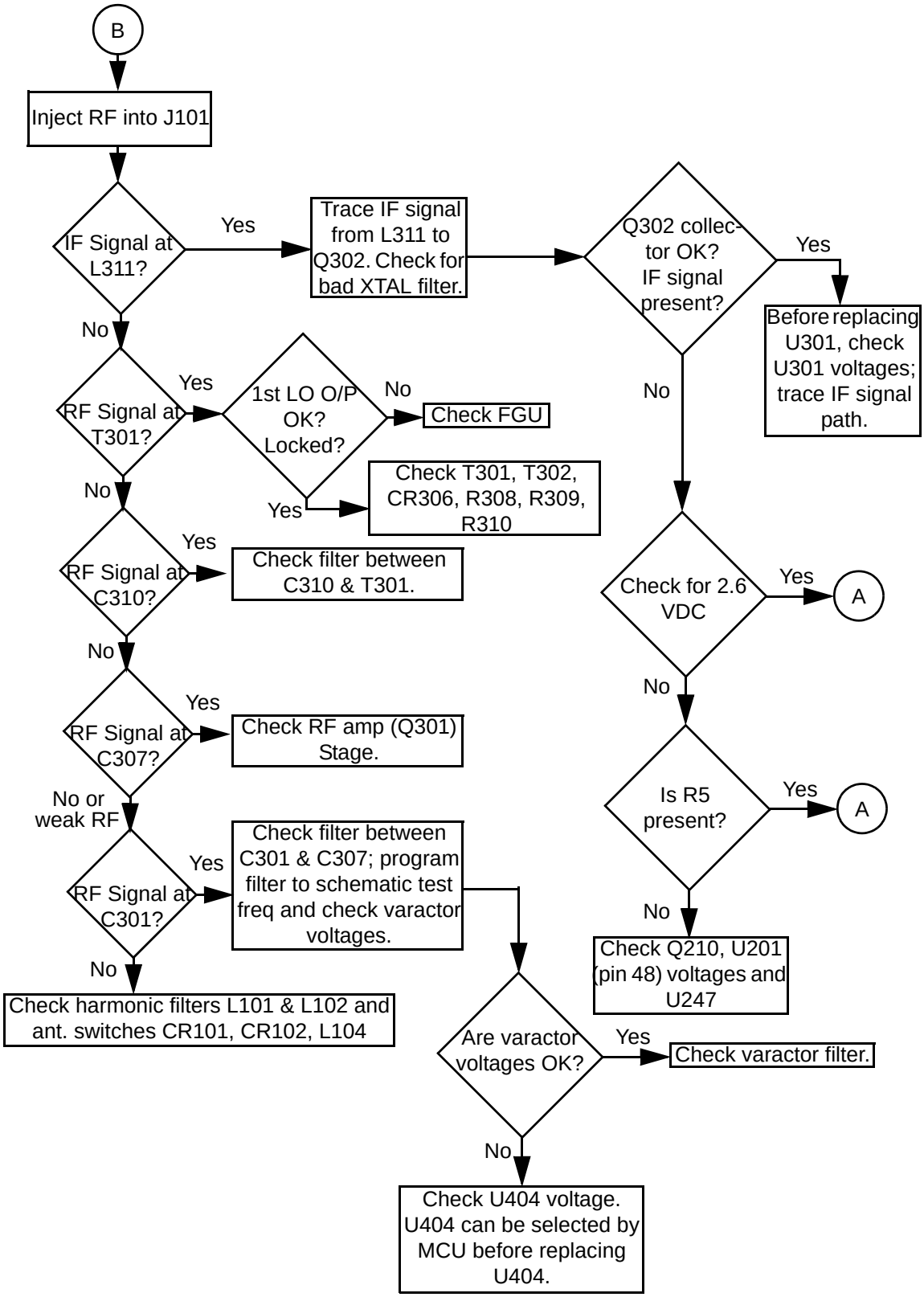
8.10.2 Troubleshooting Flow Chart for Controller for models with PCB 8486458Z03



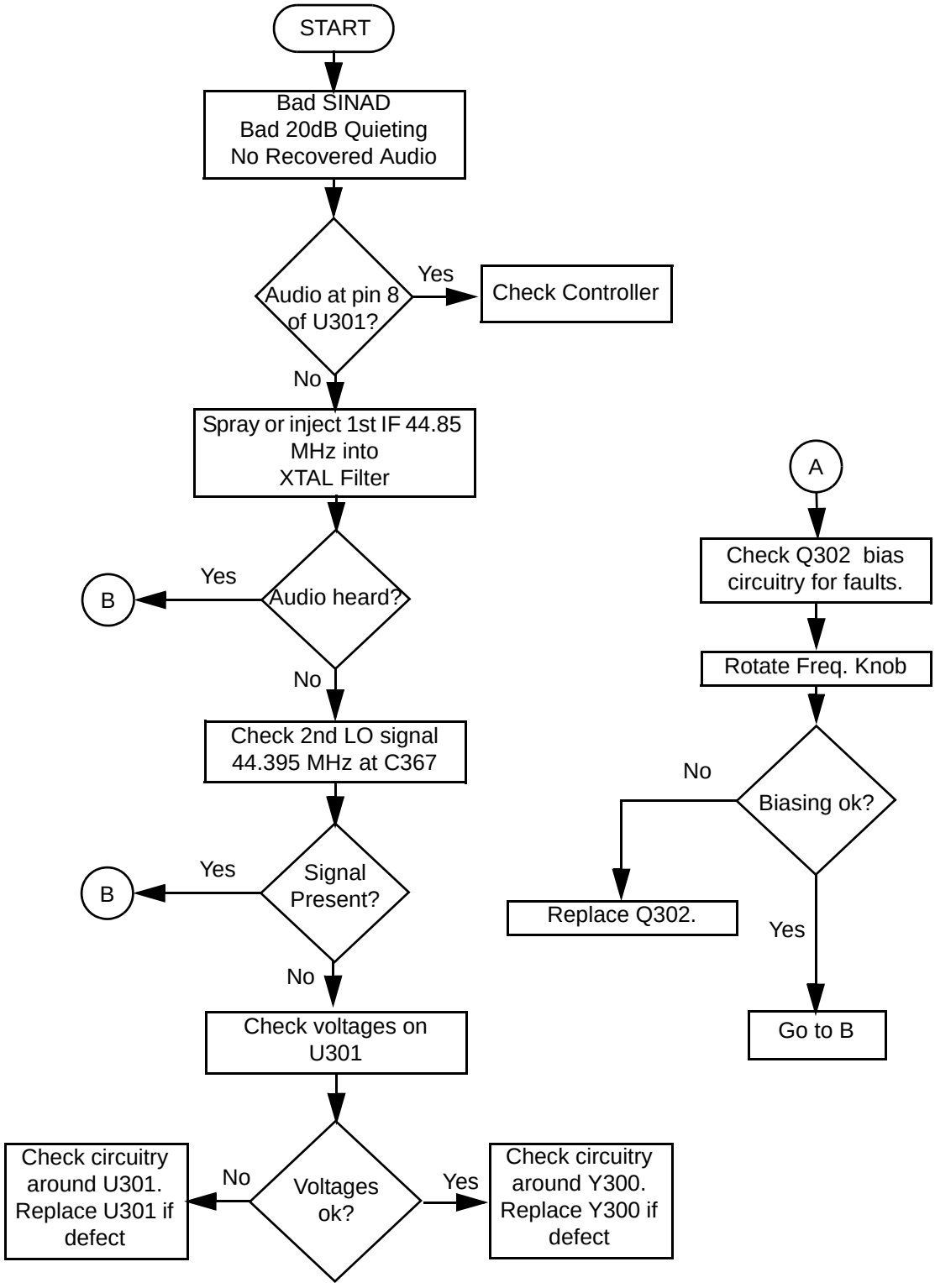
8.10.3 Troubleshooting Flow Chart for Receiver for all models except PCB 8486458Z03 (Sheet 1 of 2)



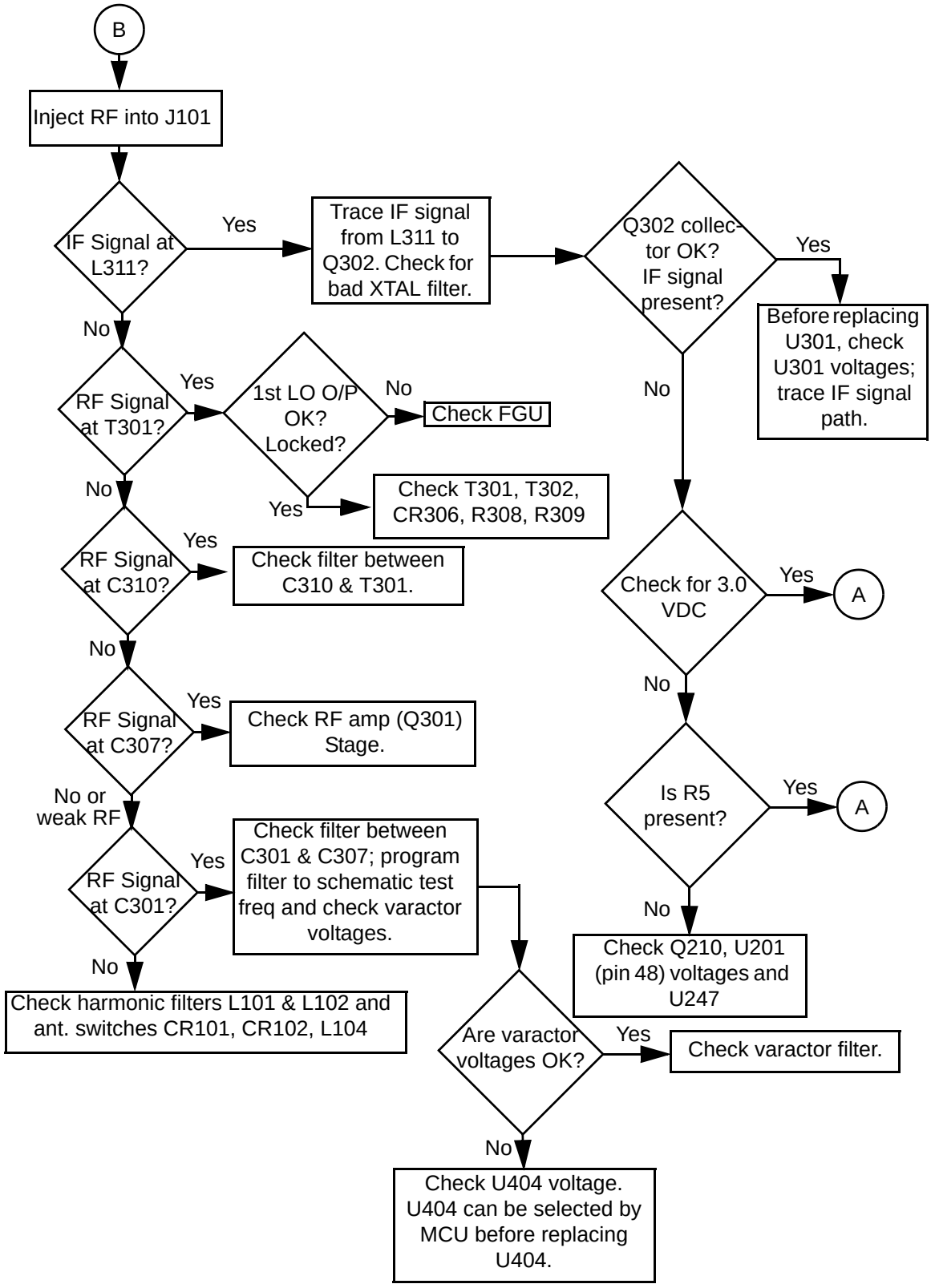
8.10.4 Troubleshooting Flow Chart for Receiver for all models except PCB 8486458Z03 (Sheet 2 of 2)



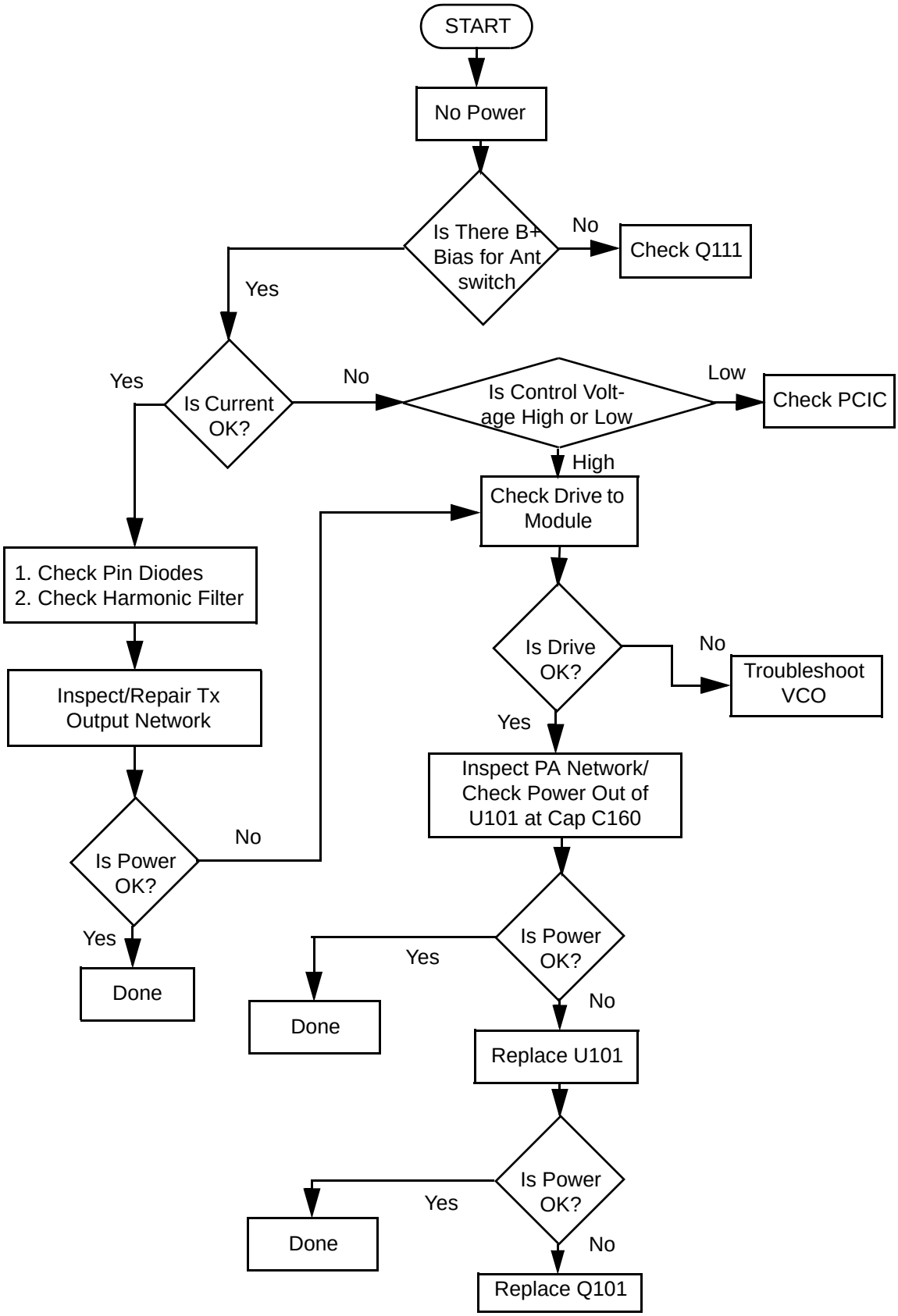
8.10.5 Troubleshooting Flow Chart for Receiver, for models with PCB 8486458Z03 (Sheet 1 of 2)



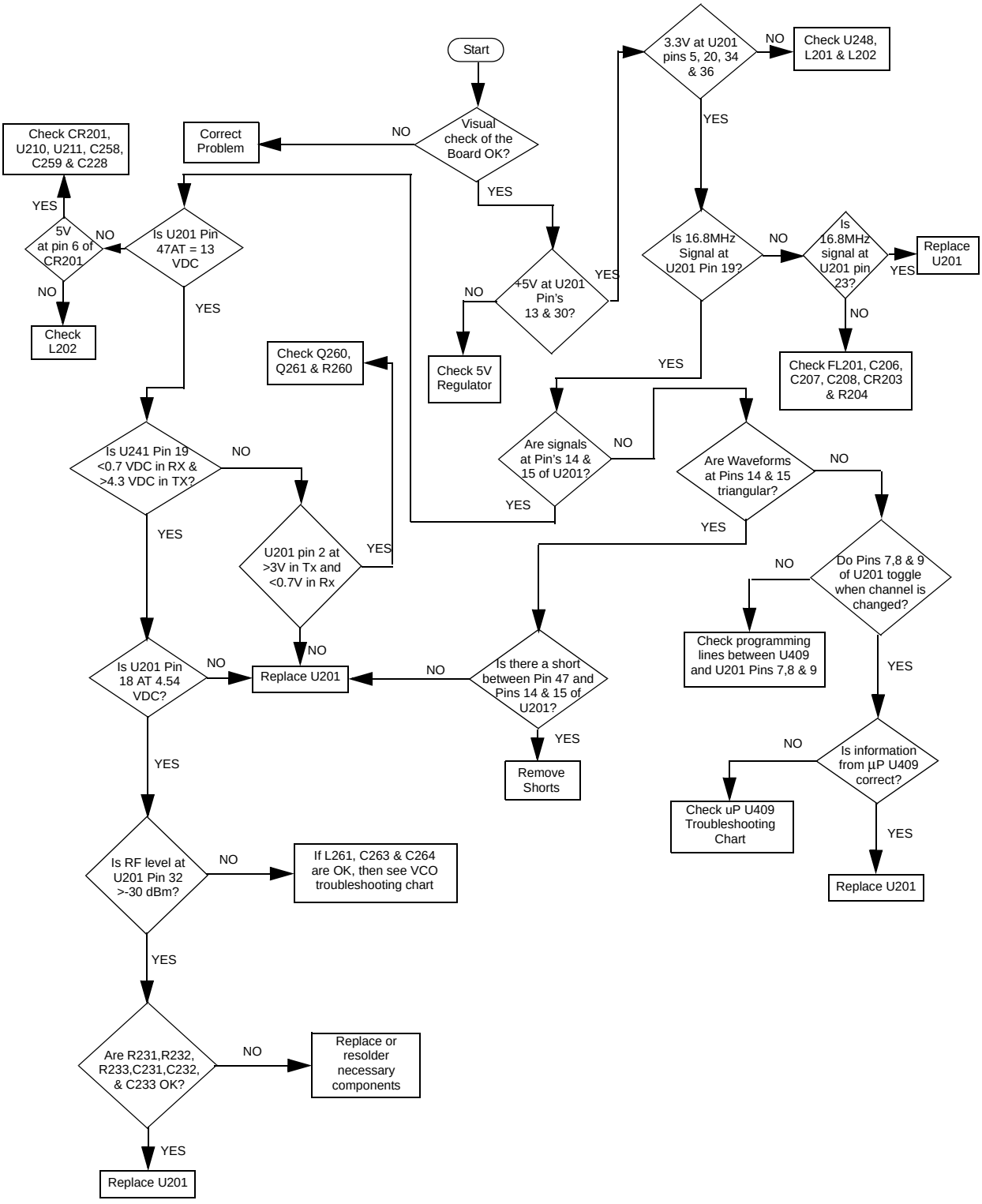
8.10.6 Troubleshooting Flow Chart for Receiver, for models with PCB 8486458Z03 (Sheet 2 of 2)



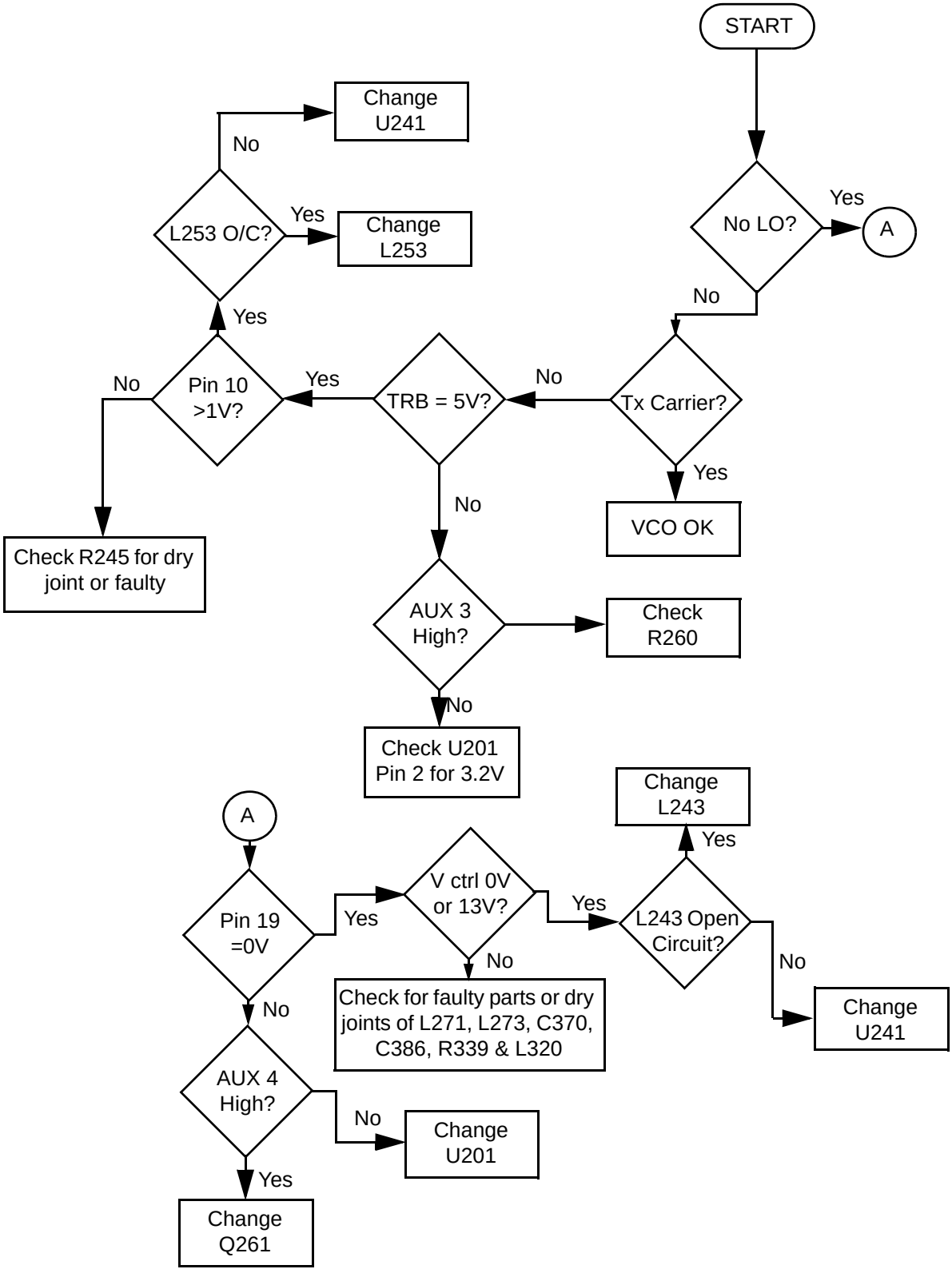
8.10.7 Troubleshooting Flow Chart for Transmitter



8.10.8 Troubleshooting Flow Chart for Synthesizer

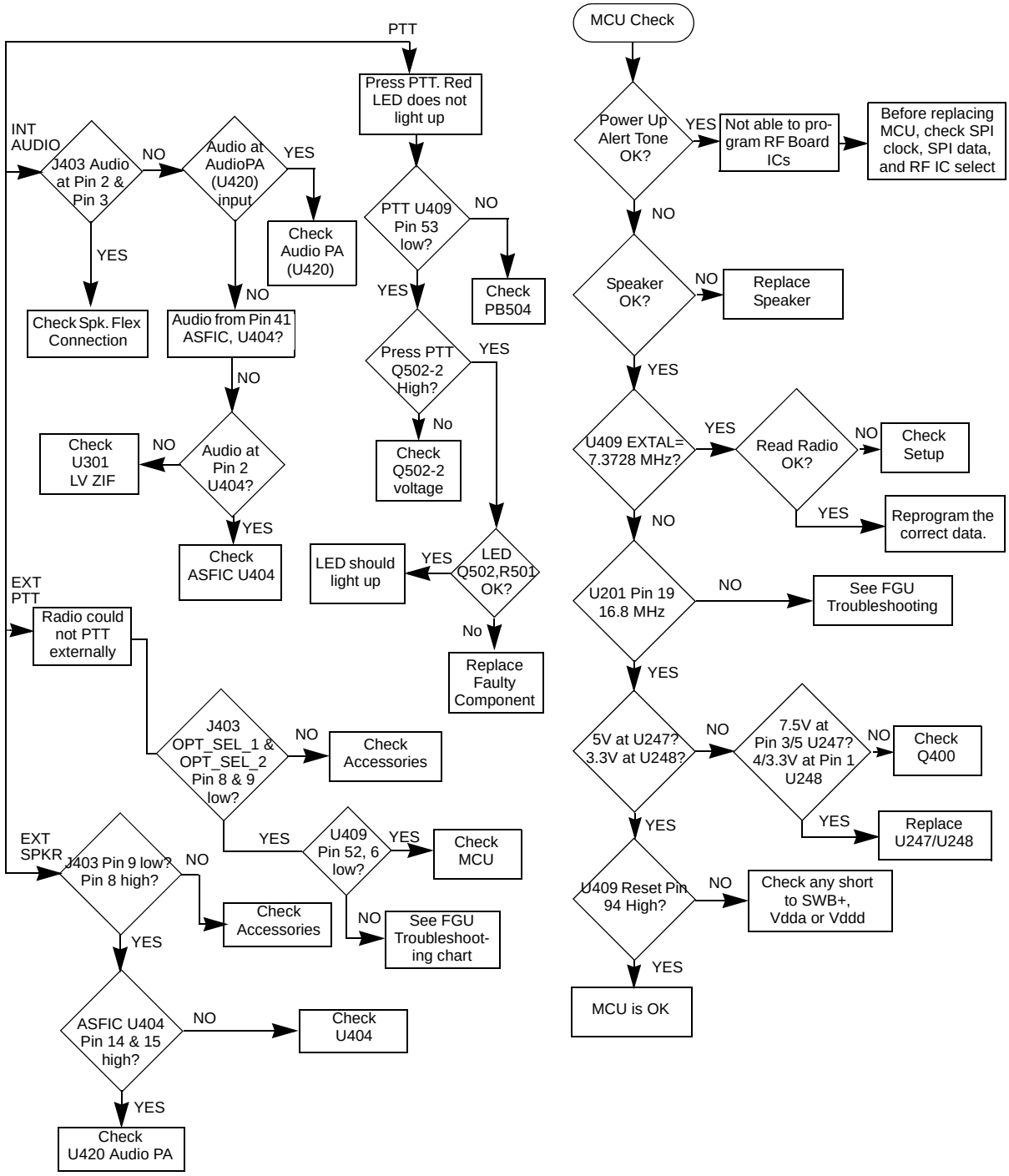


8.10.9 Troubleshooting Flow Chart for VCO

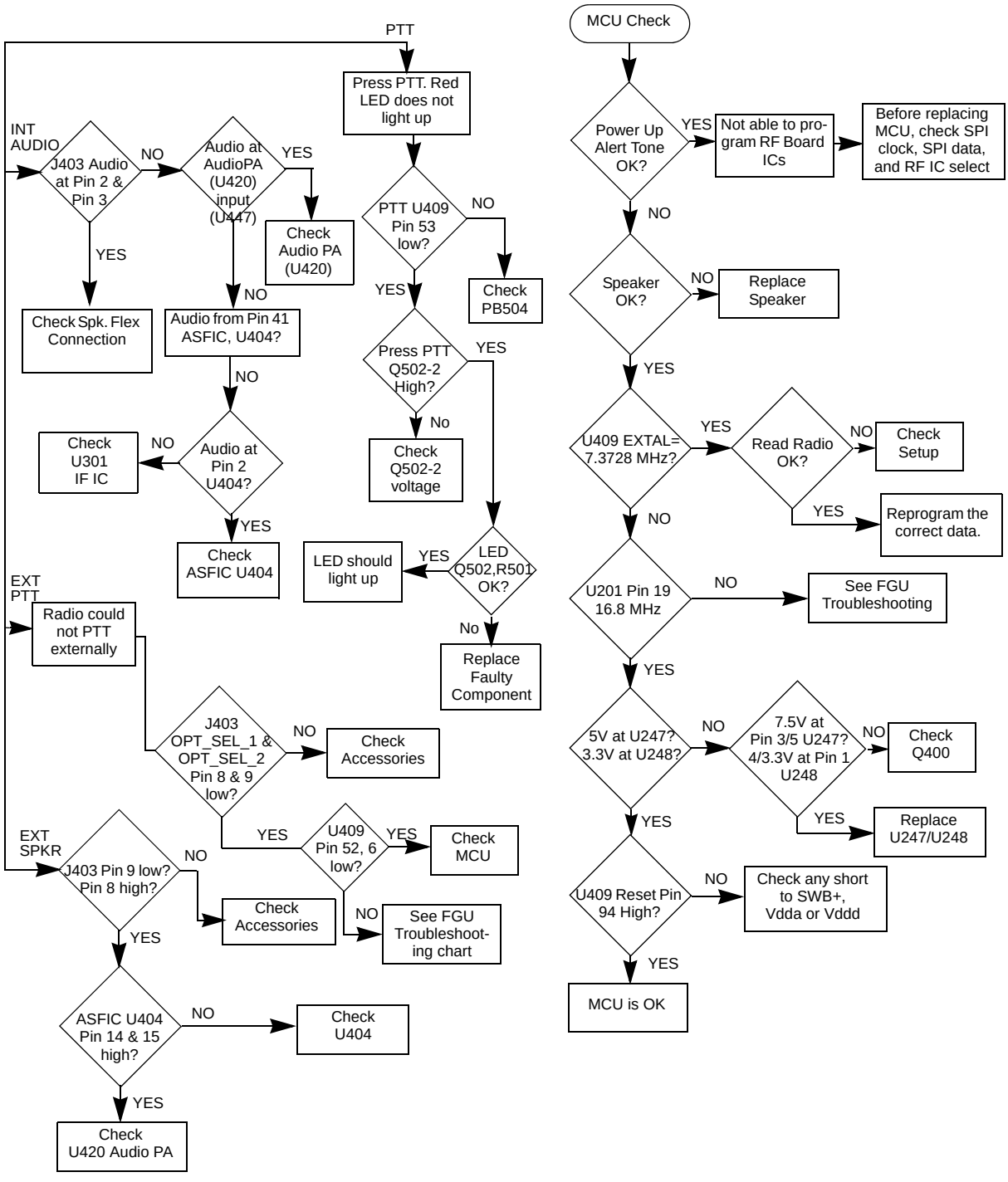


8.11 UHF Band 2 Troubleshooting Charts

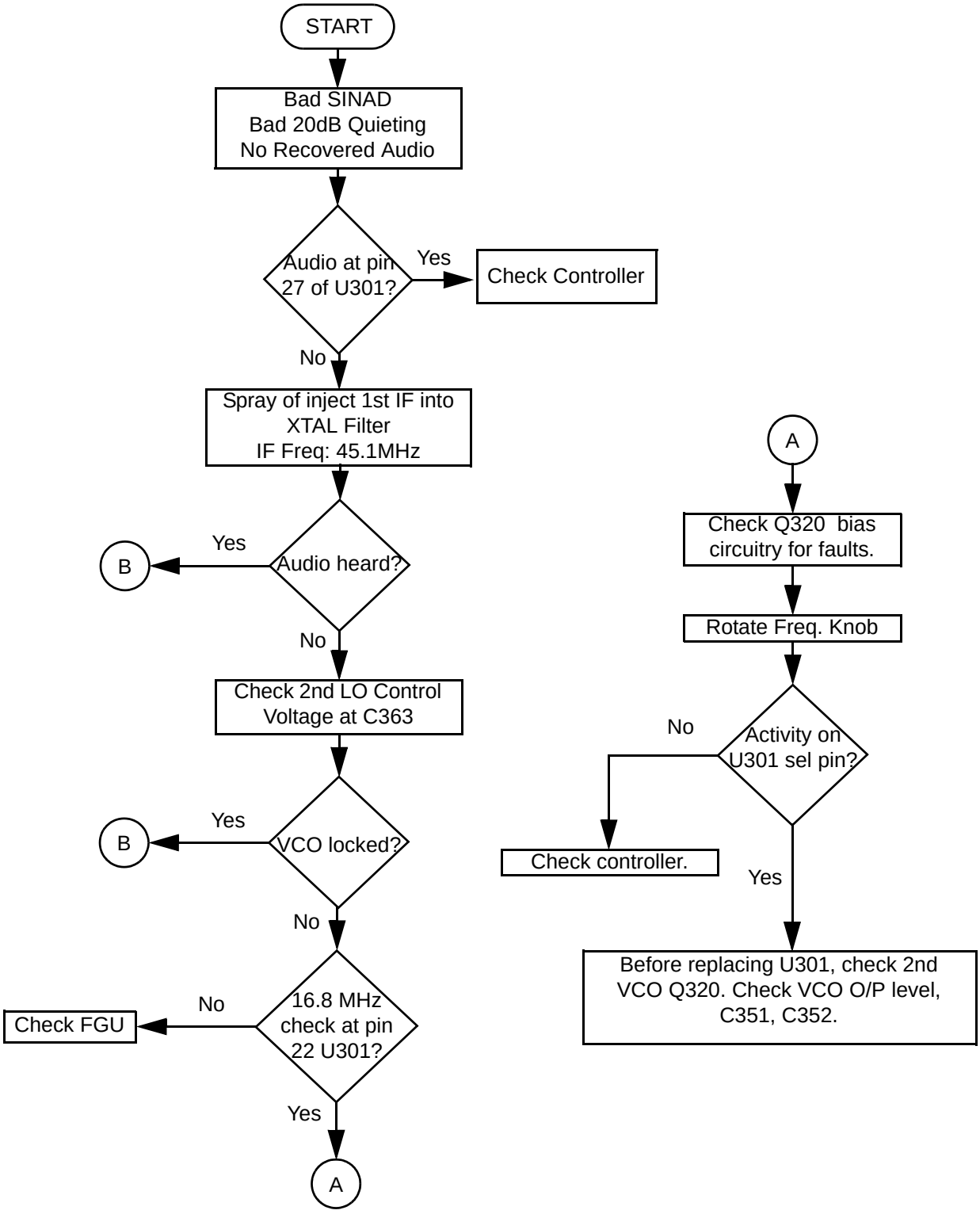
8.11.1 Troubleshooting Flow Chart for Controller for all models except those with PCB 8486686Z02



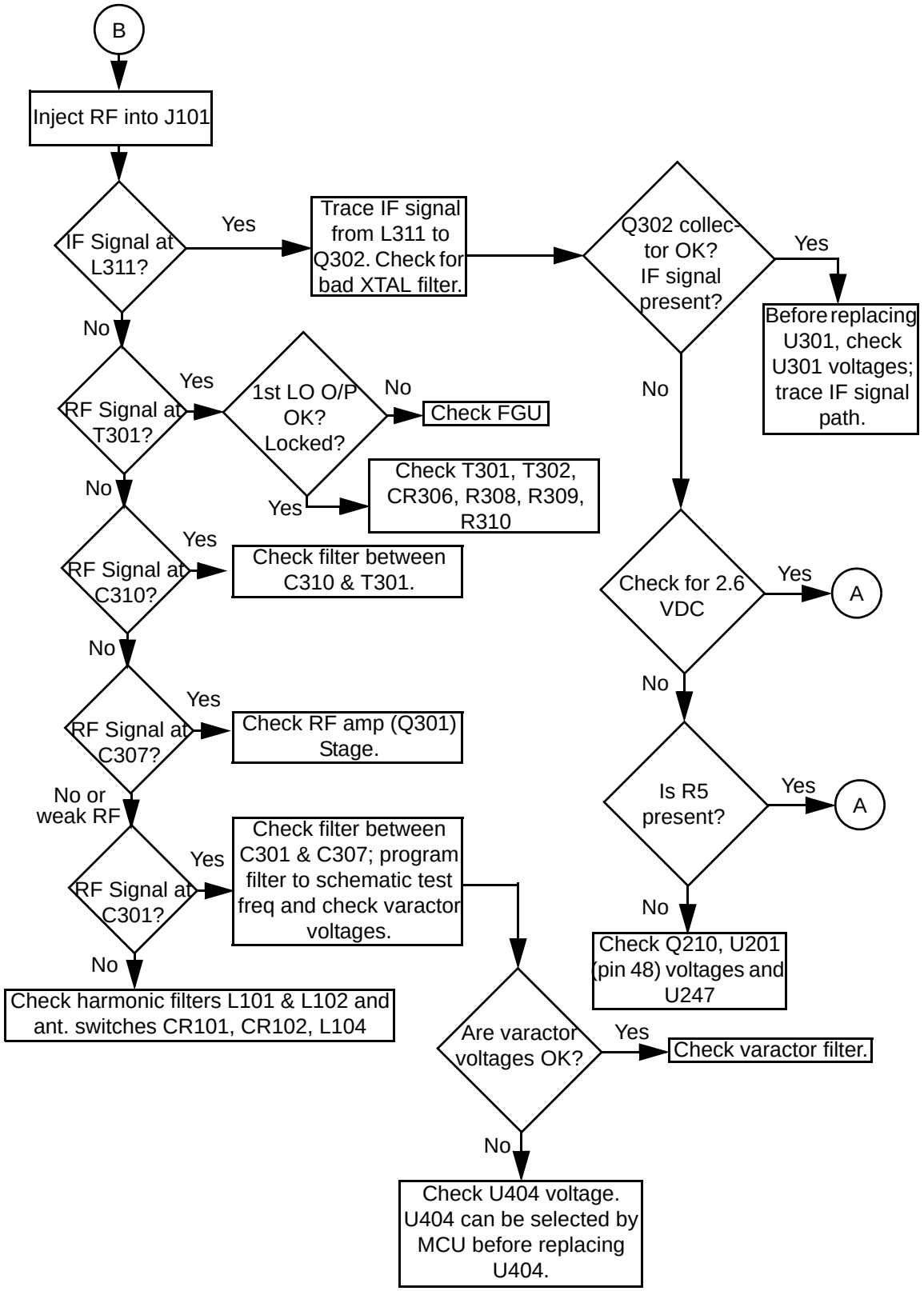
8.11.2 Troubleshooting Flow Chart for Controller for models with PCB 8486686Z02



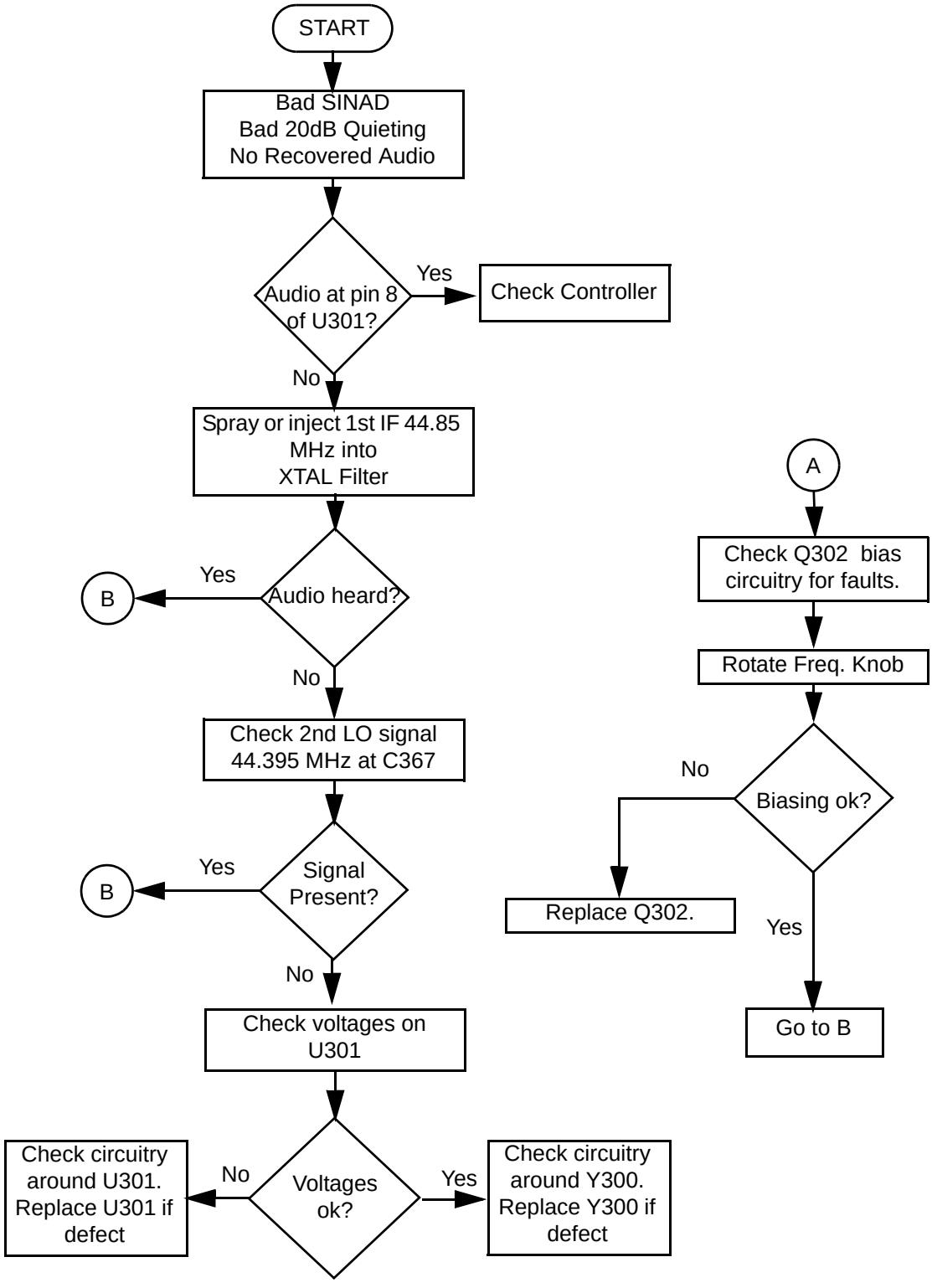
8.11.3 Troubleshooting Flow Chart for Receiver, for all models except those with PCB 8486686Z02 (Sheet 1 of 2)



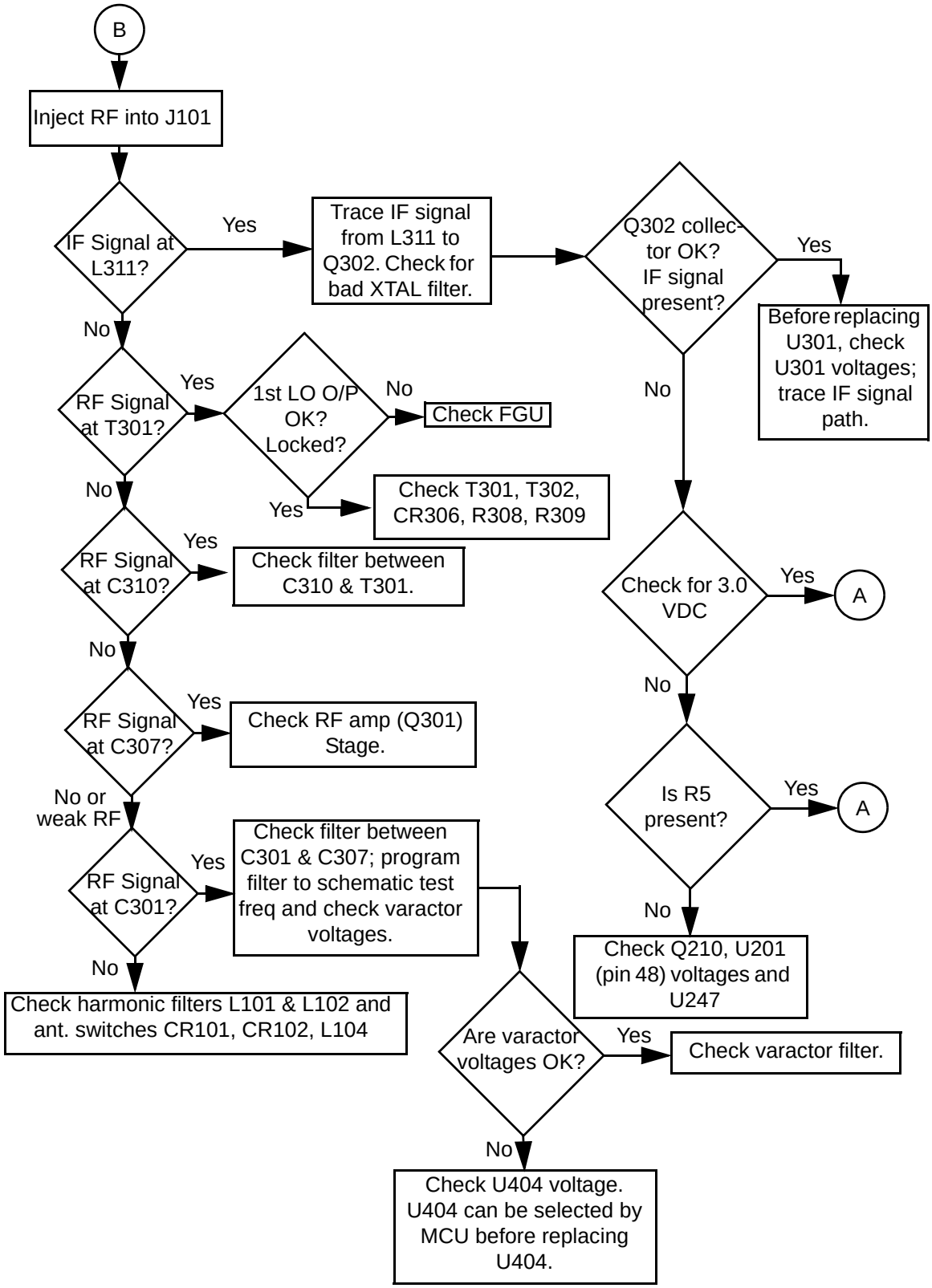
8.11.4 Troubleshooting Flow Chart for Receiver, for all models except those with PCB 8486686Z02 (Sheet 2 of 2)



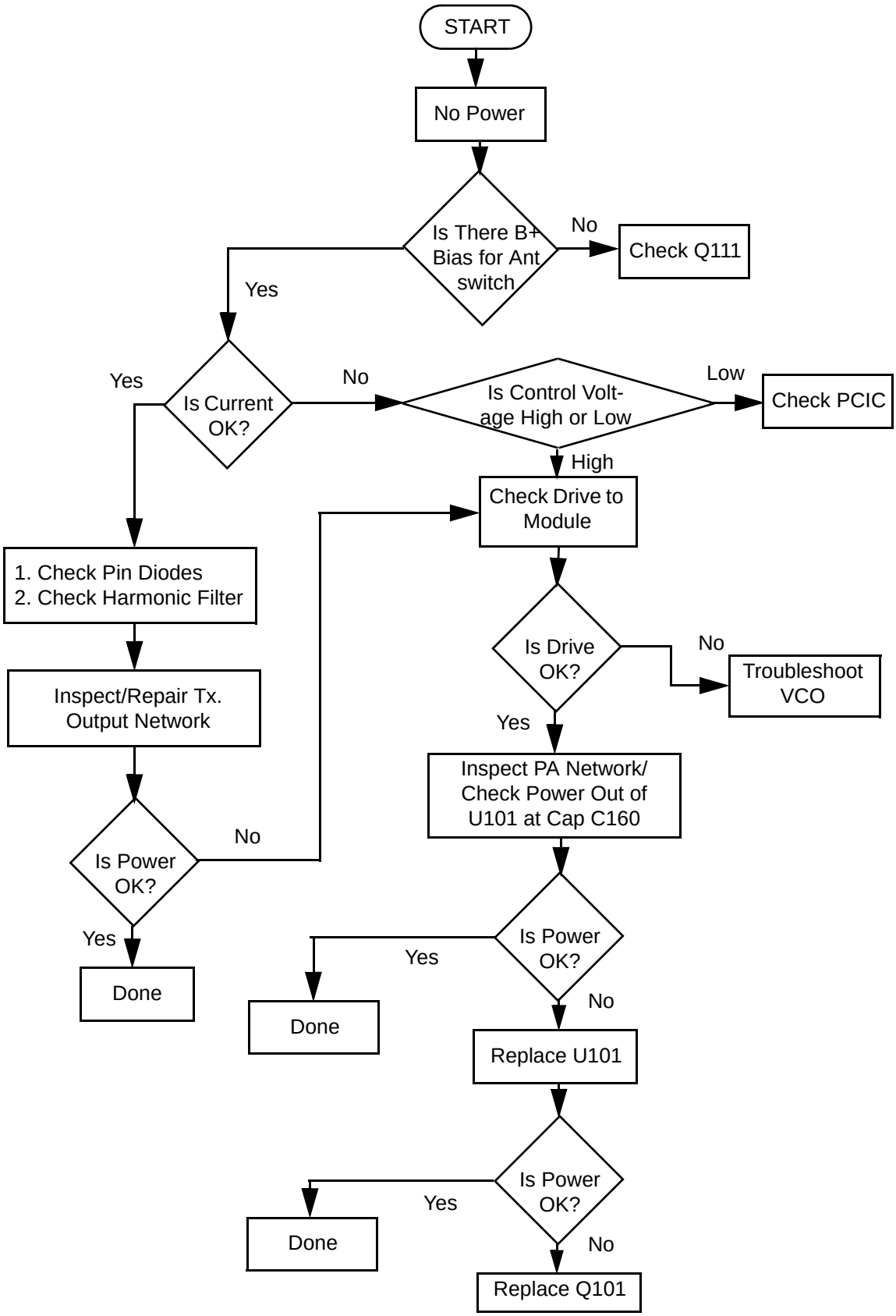
8.11.5 Troubleshooting Flow Chart for Receiver, for models with PCB 8486686Z02 (Sheet 1 of 2)



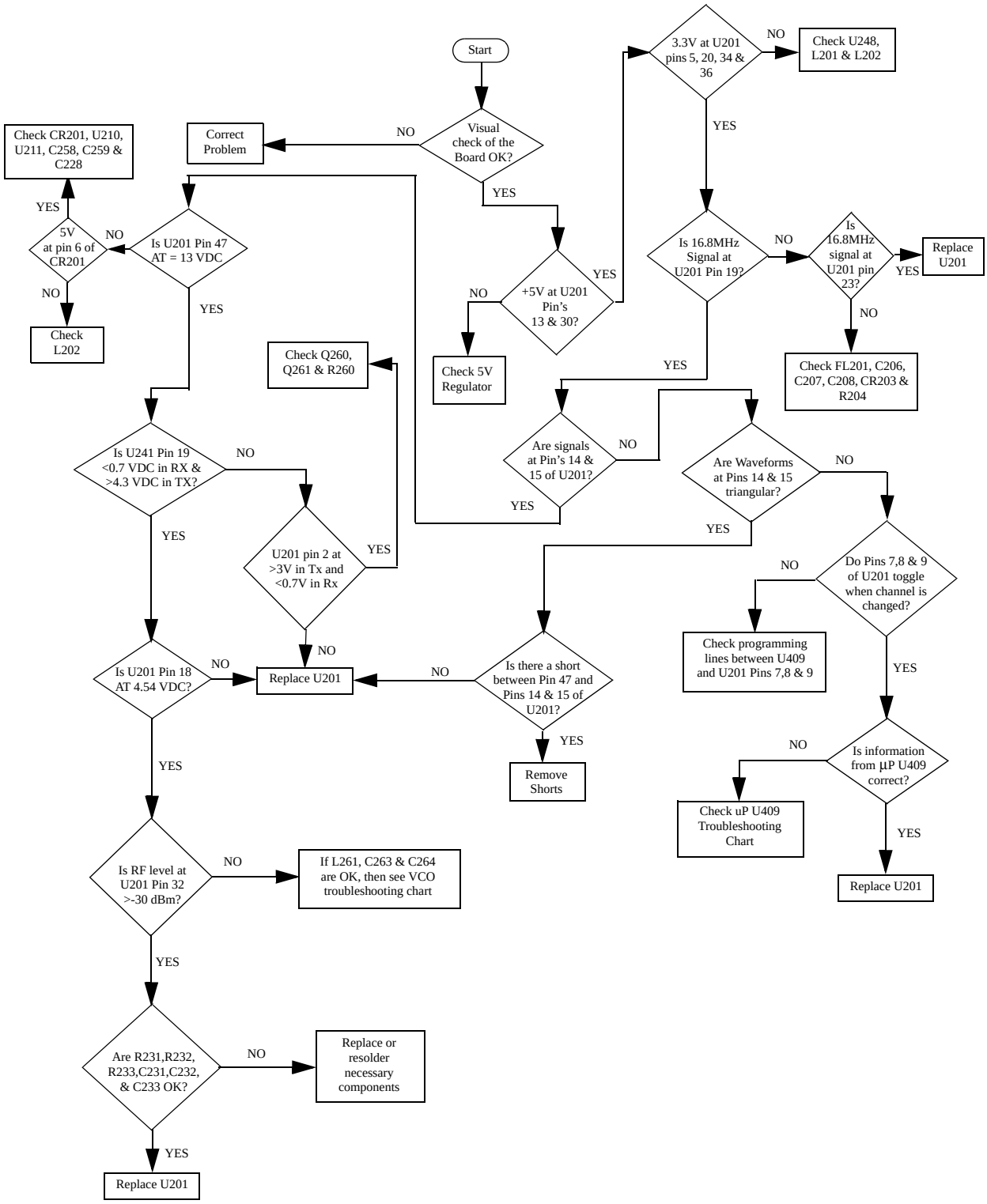
8.11.6 Troubleshooting Flow Chart for Receiver, for models with PCB 8486686Z02 (Sheet 2 of 2)



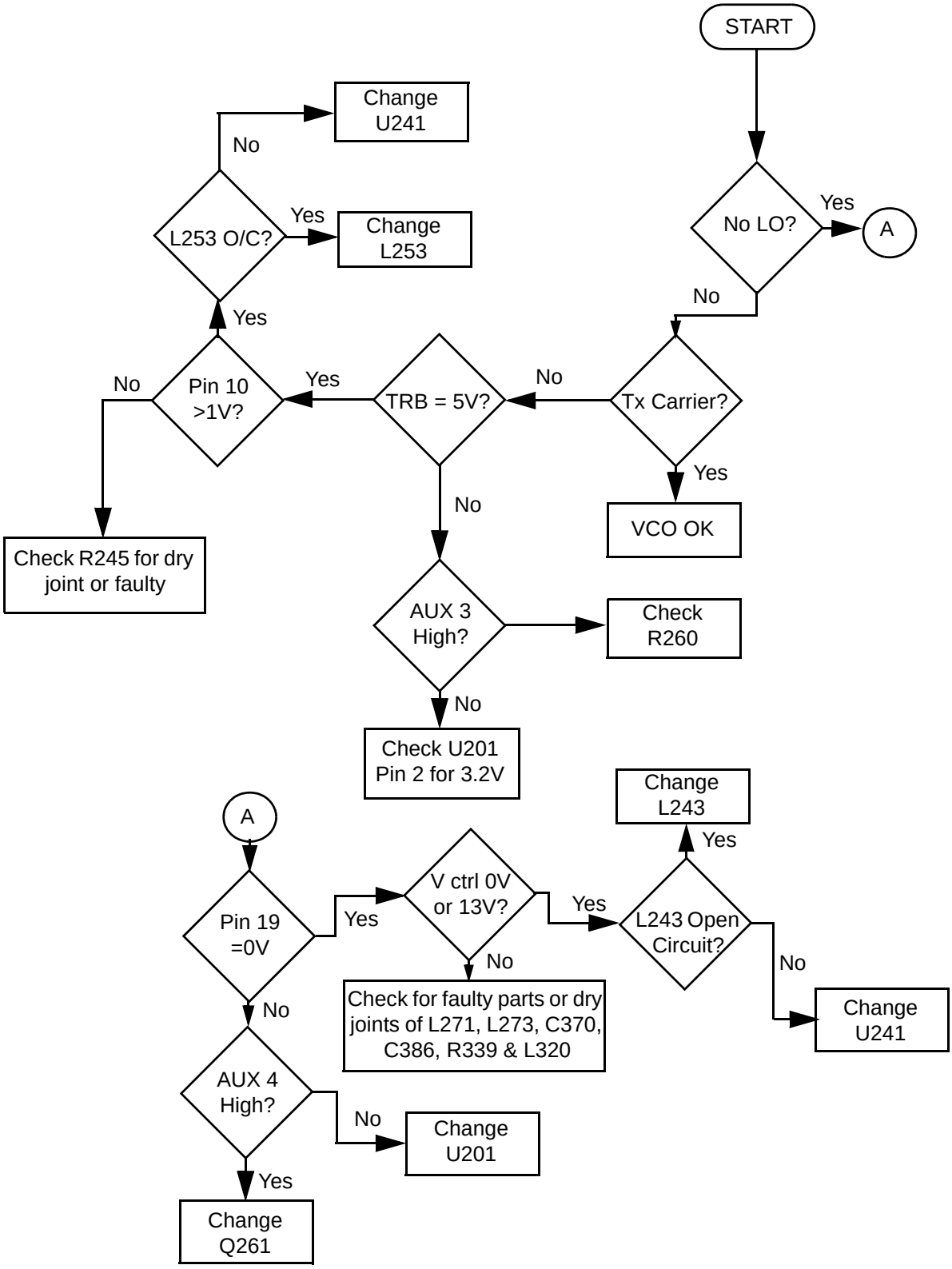
8.11.7 Troubleshooting Flow Chart for Transmitter



8.11.8 Troubleshooting Flow Chart for Synthesizer

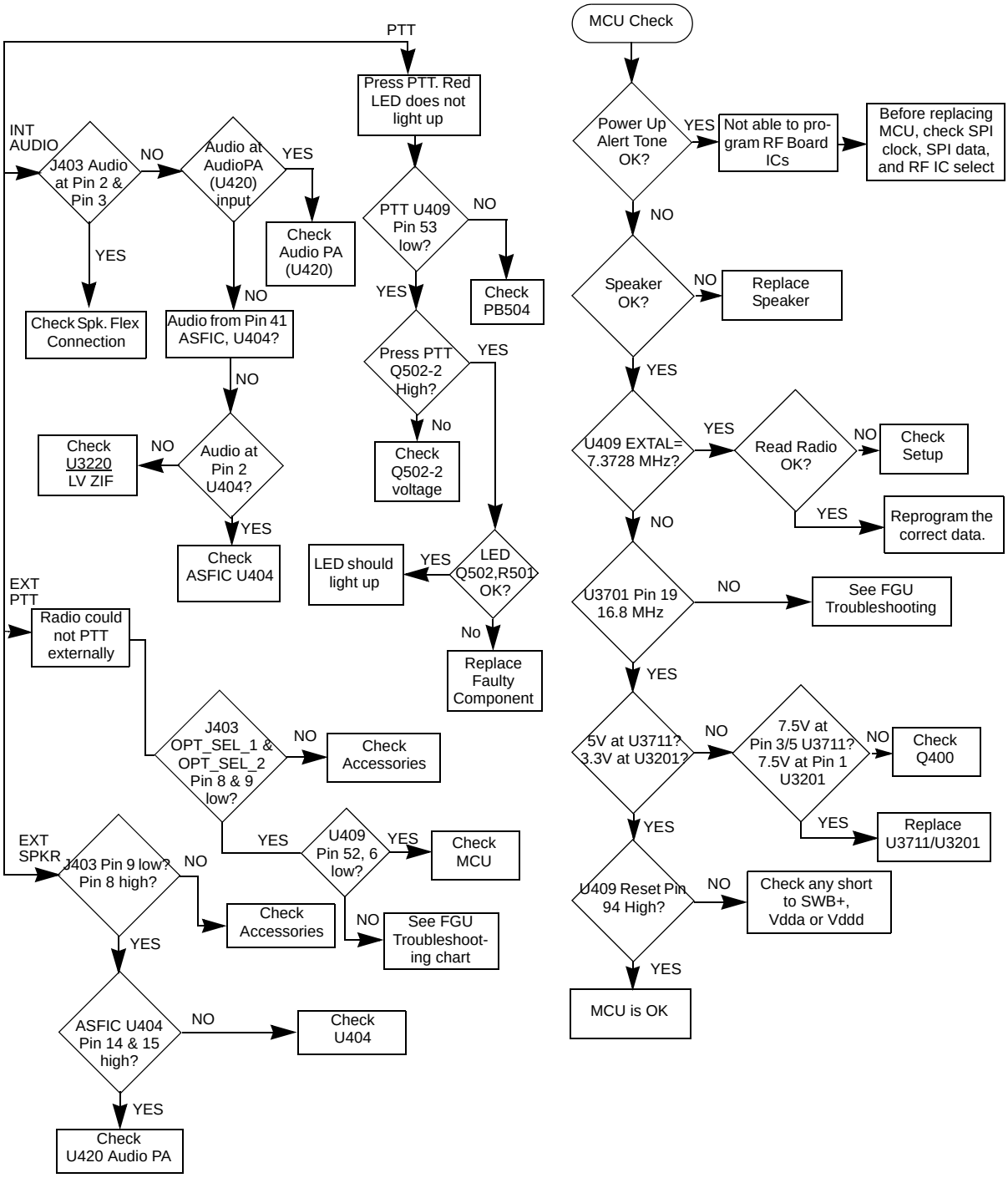


8.11.9 Troubleshooting Flow Chart for VCO

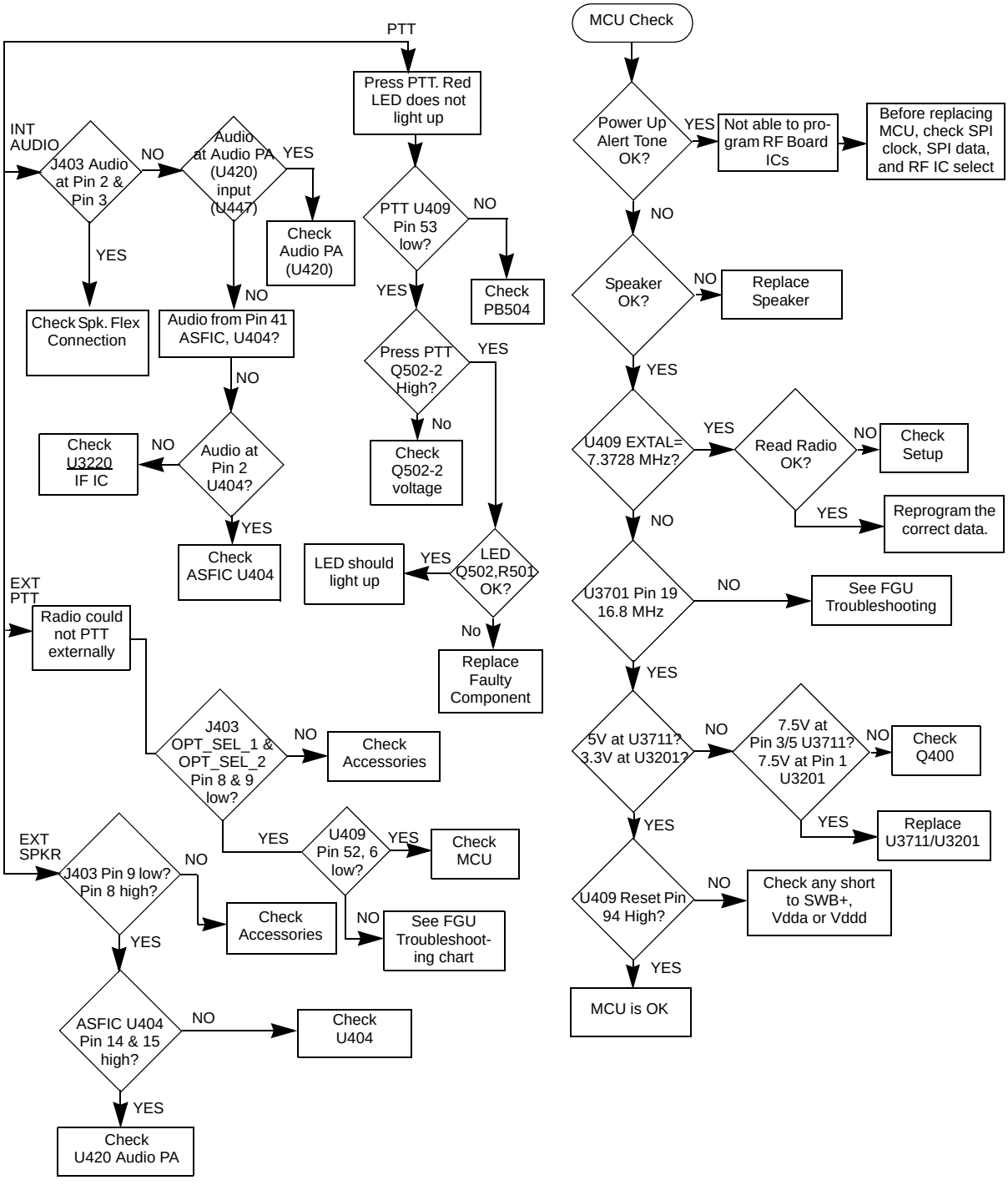


8.12 VHF Troubleshooting Charts

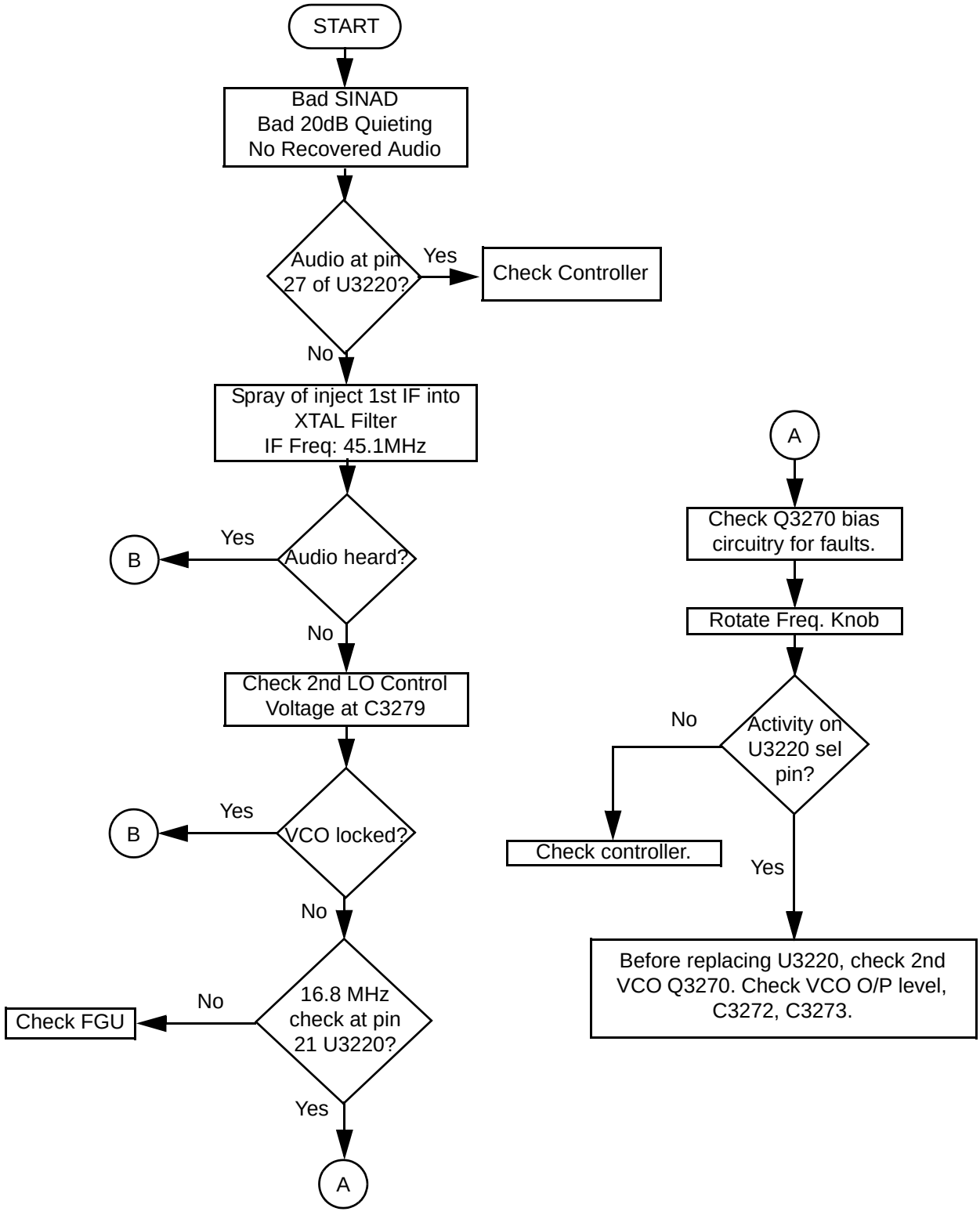
8.12.1 Troubleshooting Flow Chart for Controller for all models except those with PCB 8486473Z04



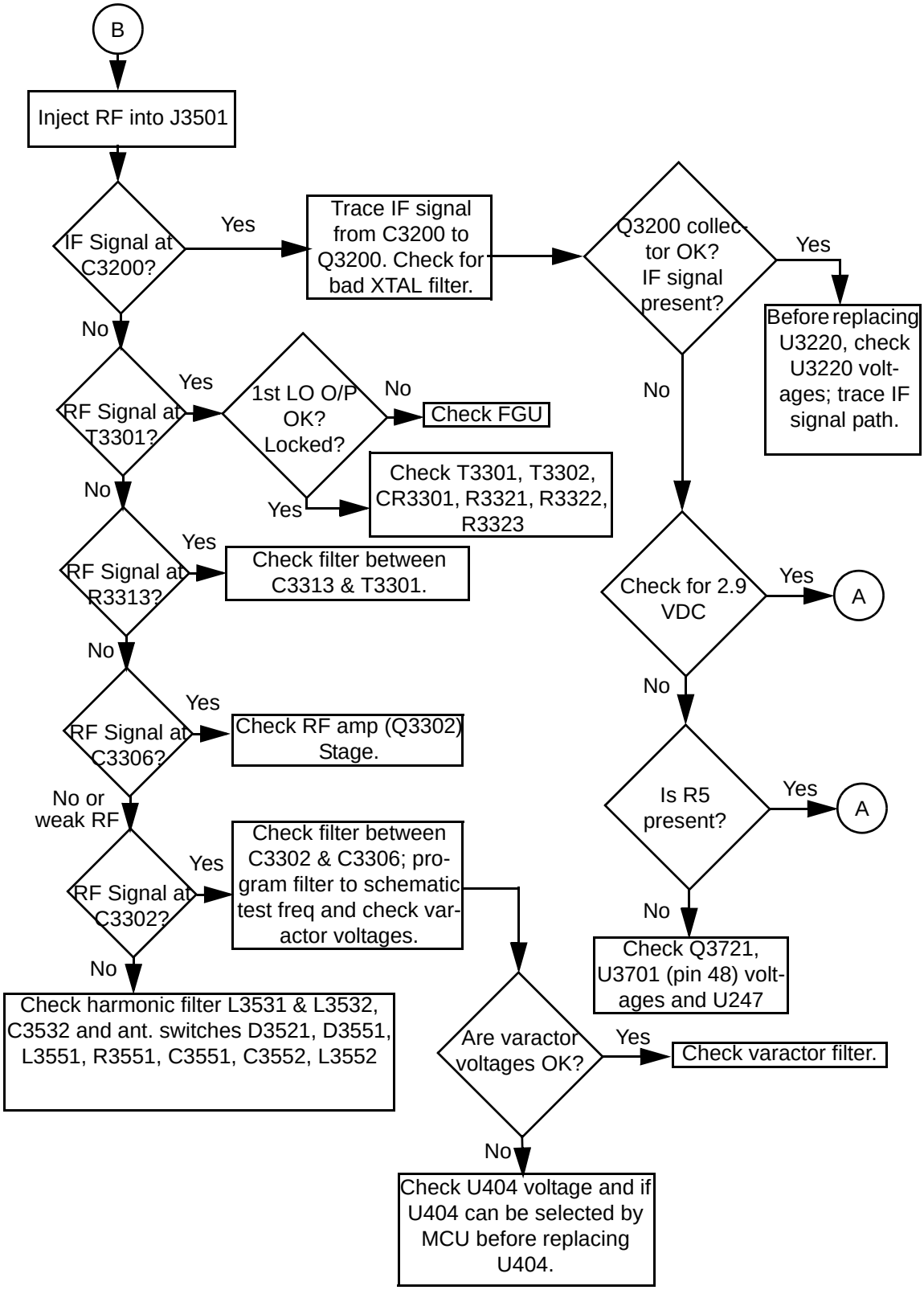
8.12.2 Troubleshooting Flow Chart for Controller for models with PCB 8486473Z04



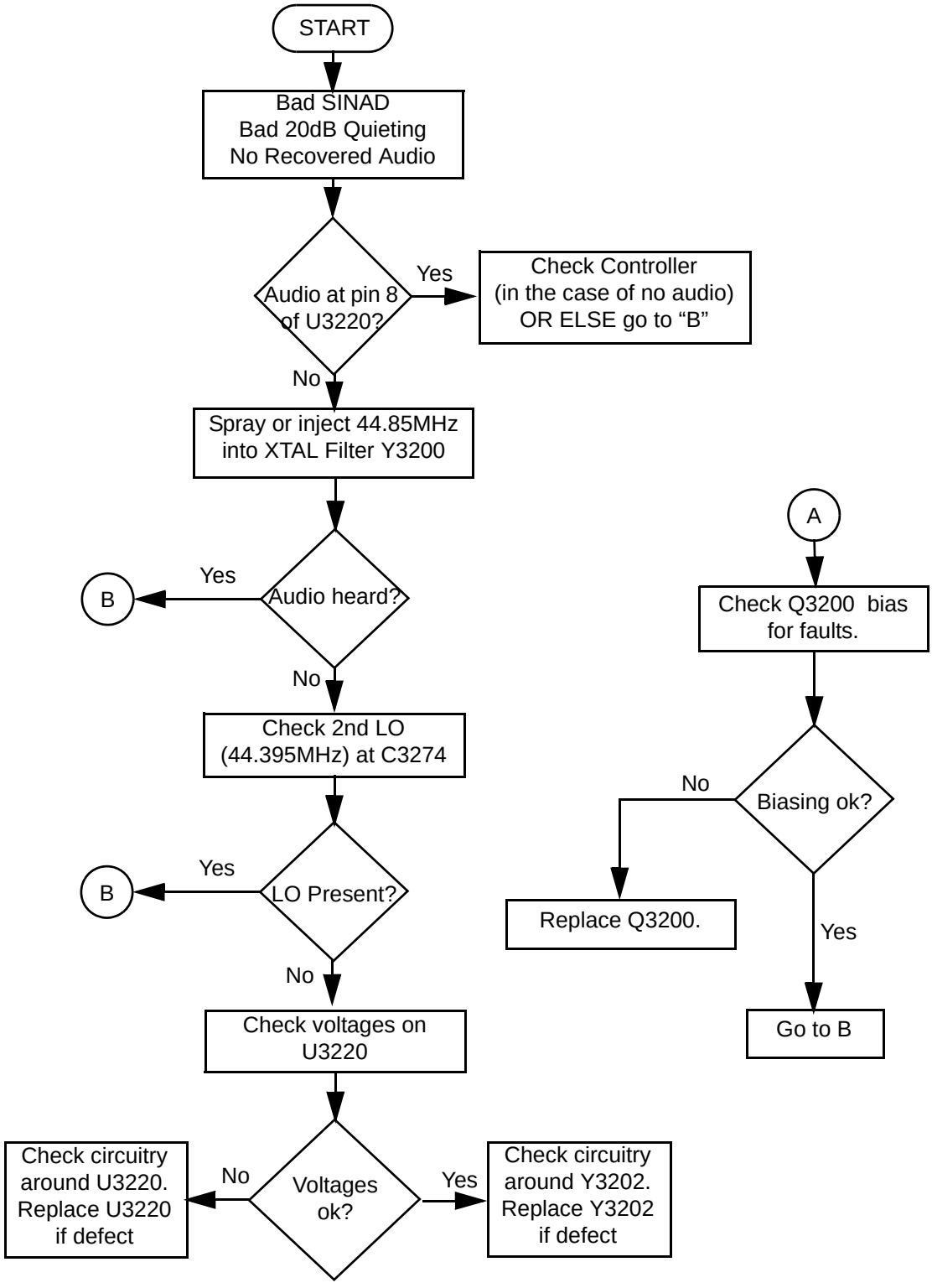
8.12.3 Troubleshooting Flow Chart for Receiver, for all models except those with PCB 8486473Z04 (Sheet 1 of 2)



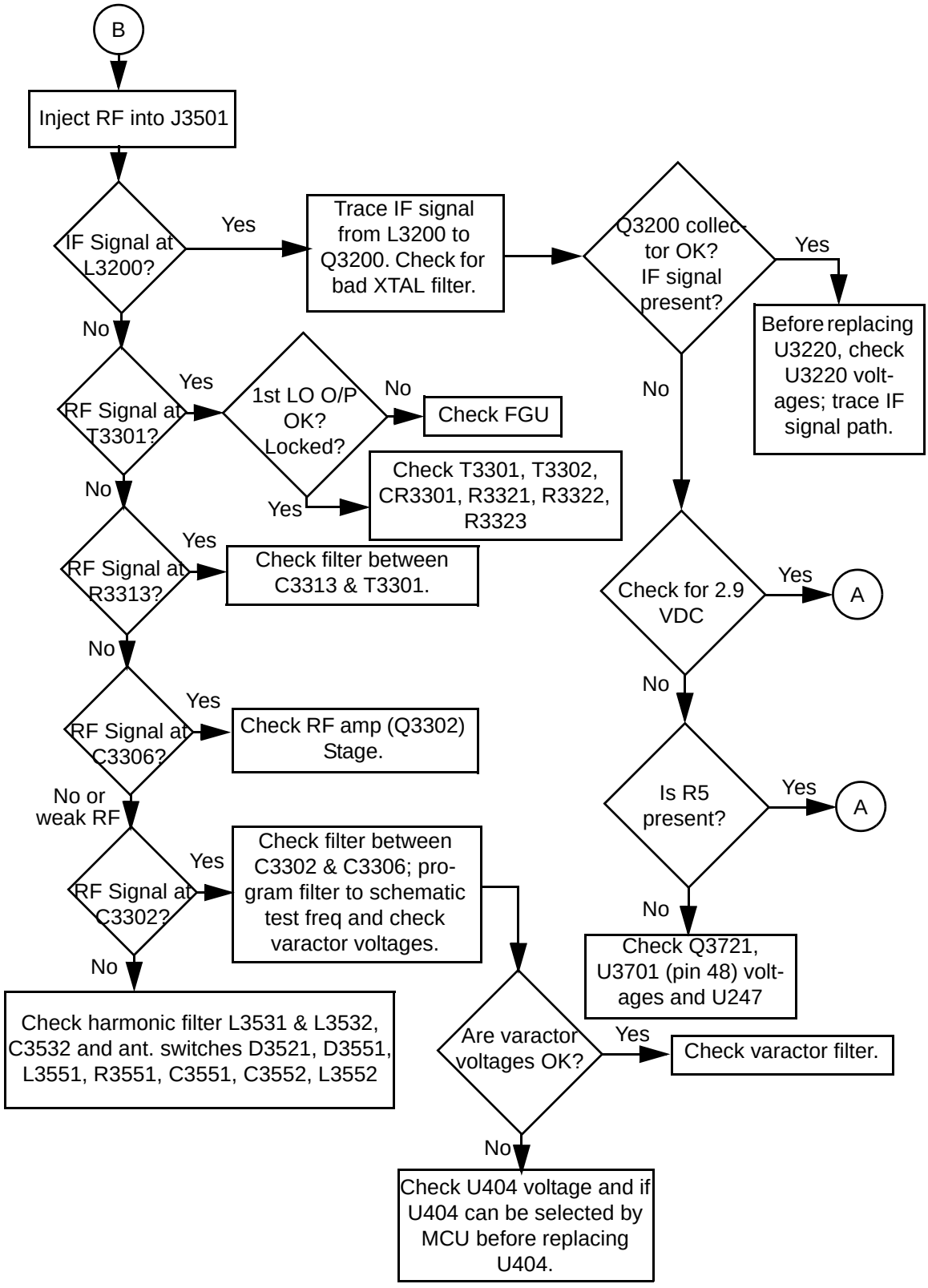
8.12.4 Troubleshooting Flow Chart for Receiver, for all models except those with PCB 8486473Z04 (Sheet 2 of 2)



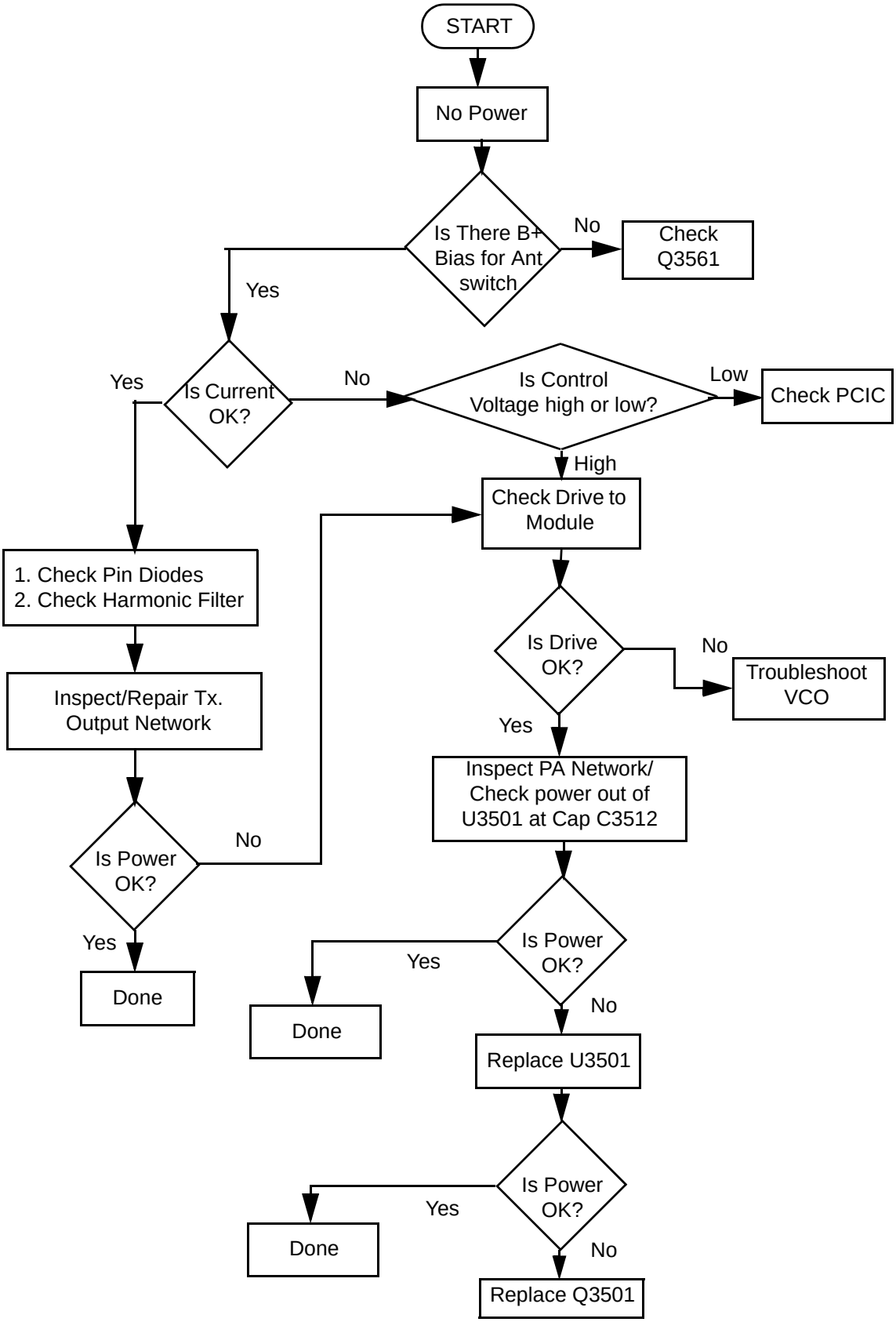
8.12.5 Troubleshooting Flow Chart for Receiver for models with PCB 8486473Z04 (Sheet 1 of 2)



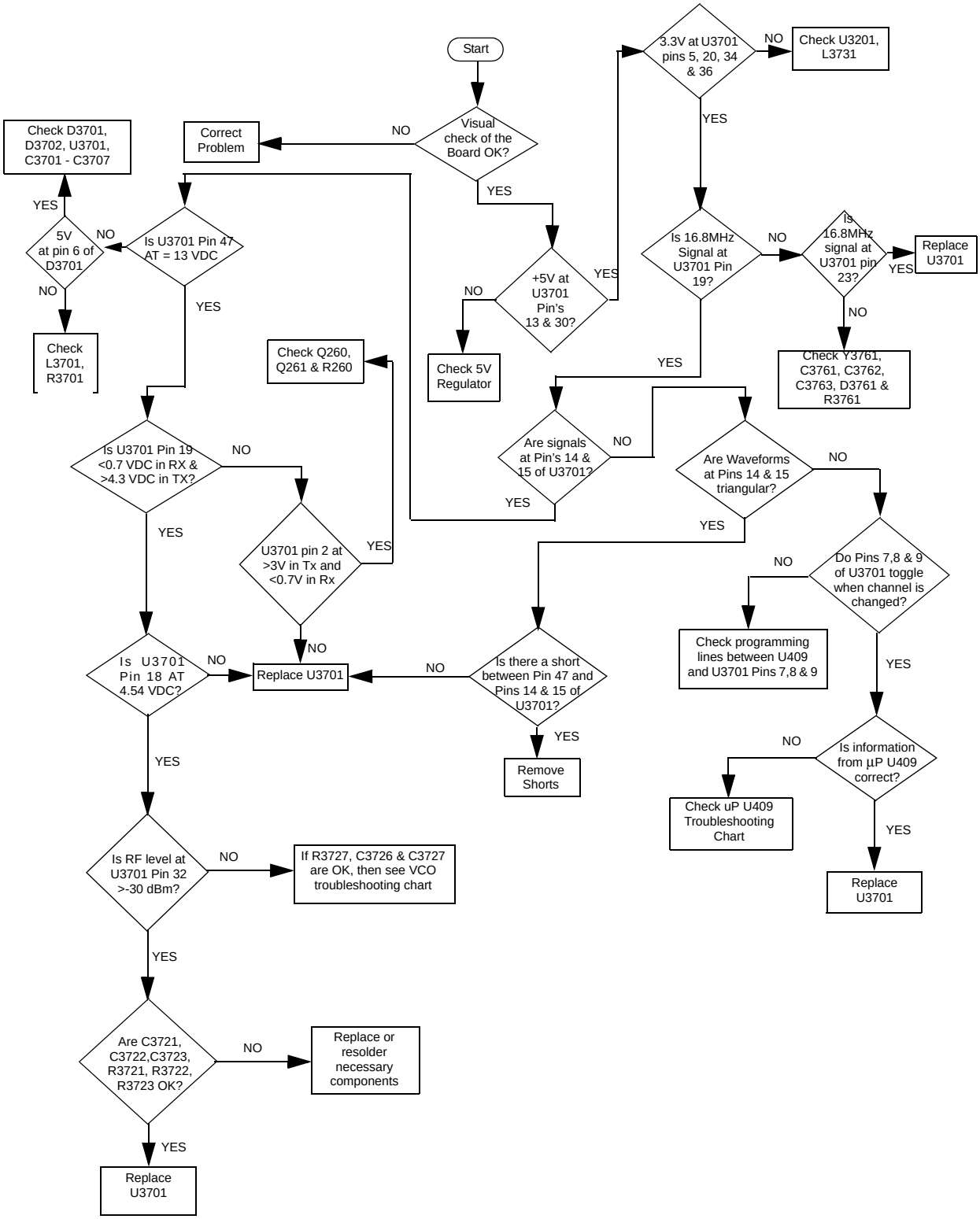
8.12.6 Troubleshooting Flow Chart for Receiver for models with PCB 8486473Z04 (Sheet 2 of 2)



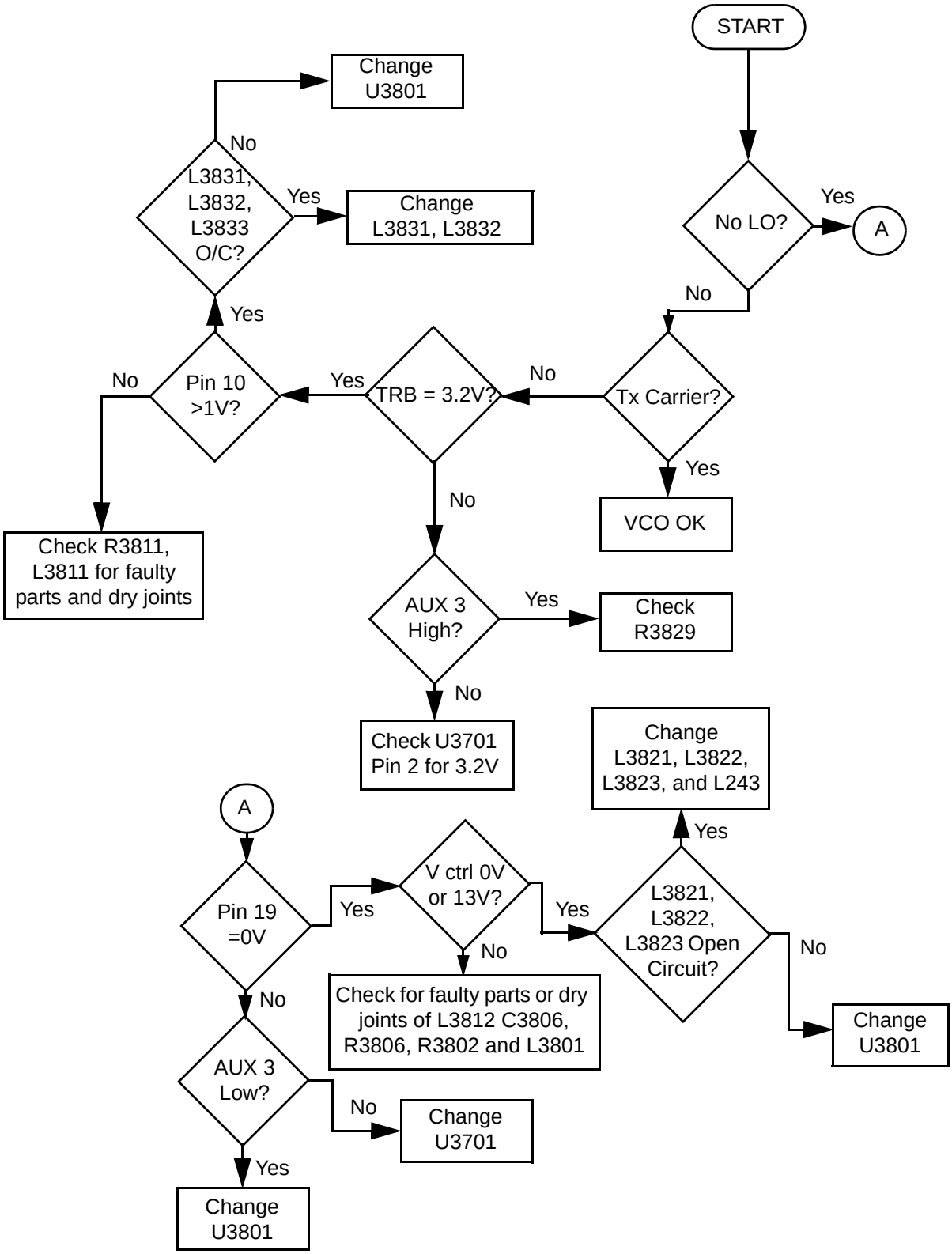
8.12.7 Troubleshooting Flow Chart for Transmitter



8.12.8 Troubleshooting Flow Chart for Synthesizer

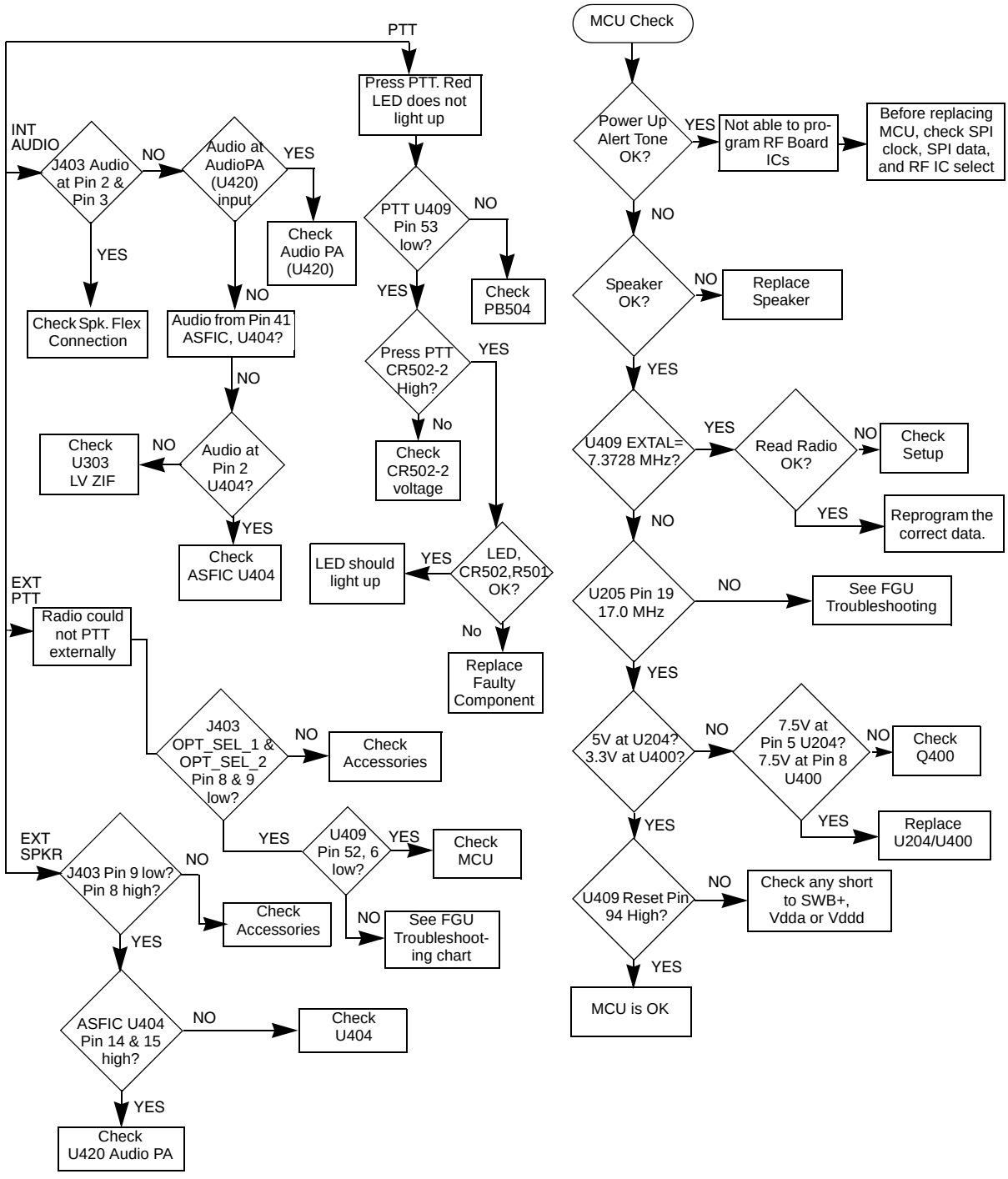


8.12.9 Troubleshooting Flow Chart for VCO

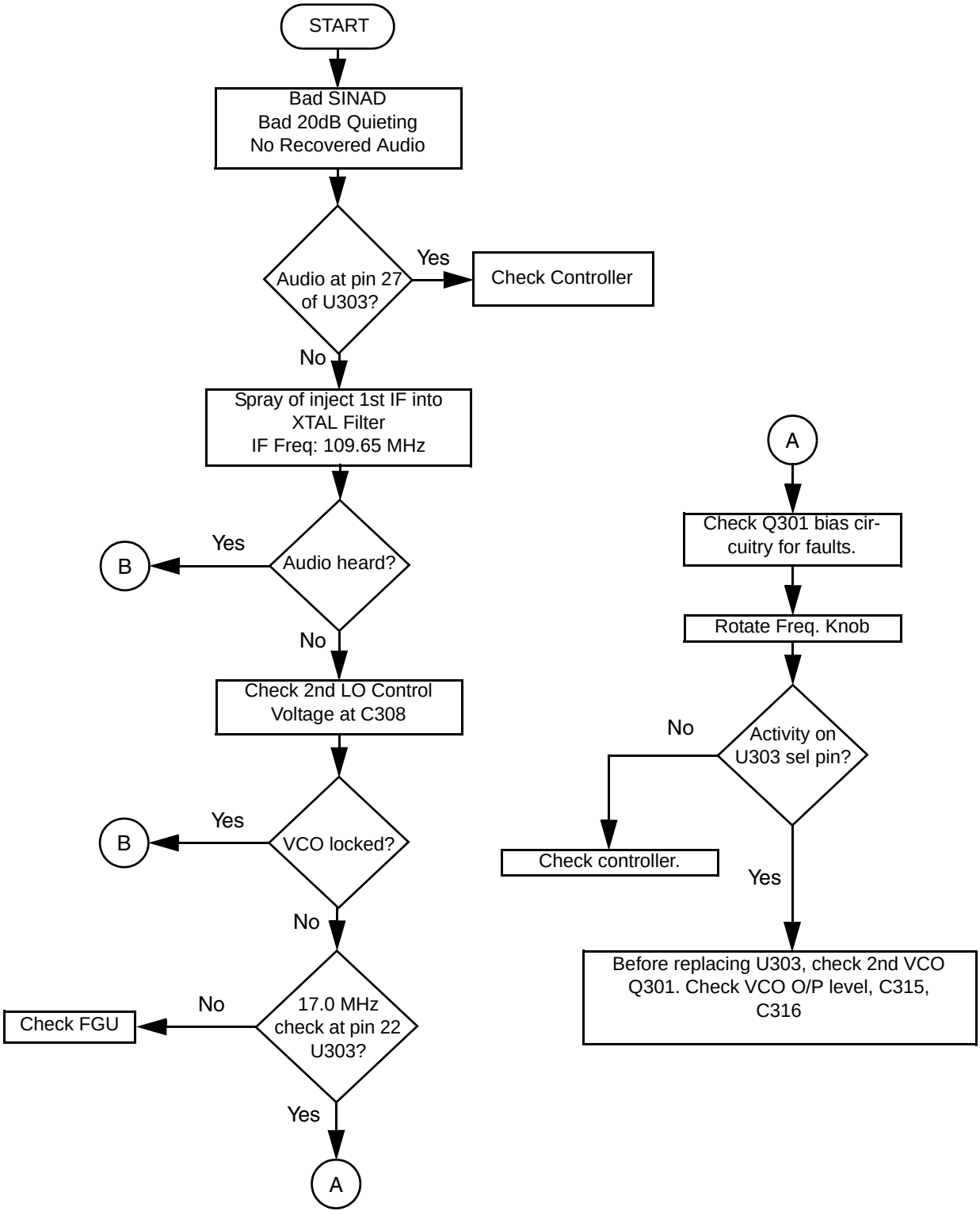


8.13 Low Band Troubleshooting Charts

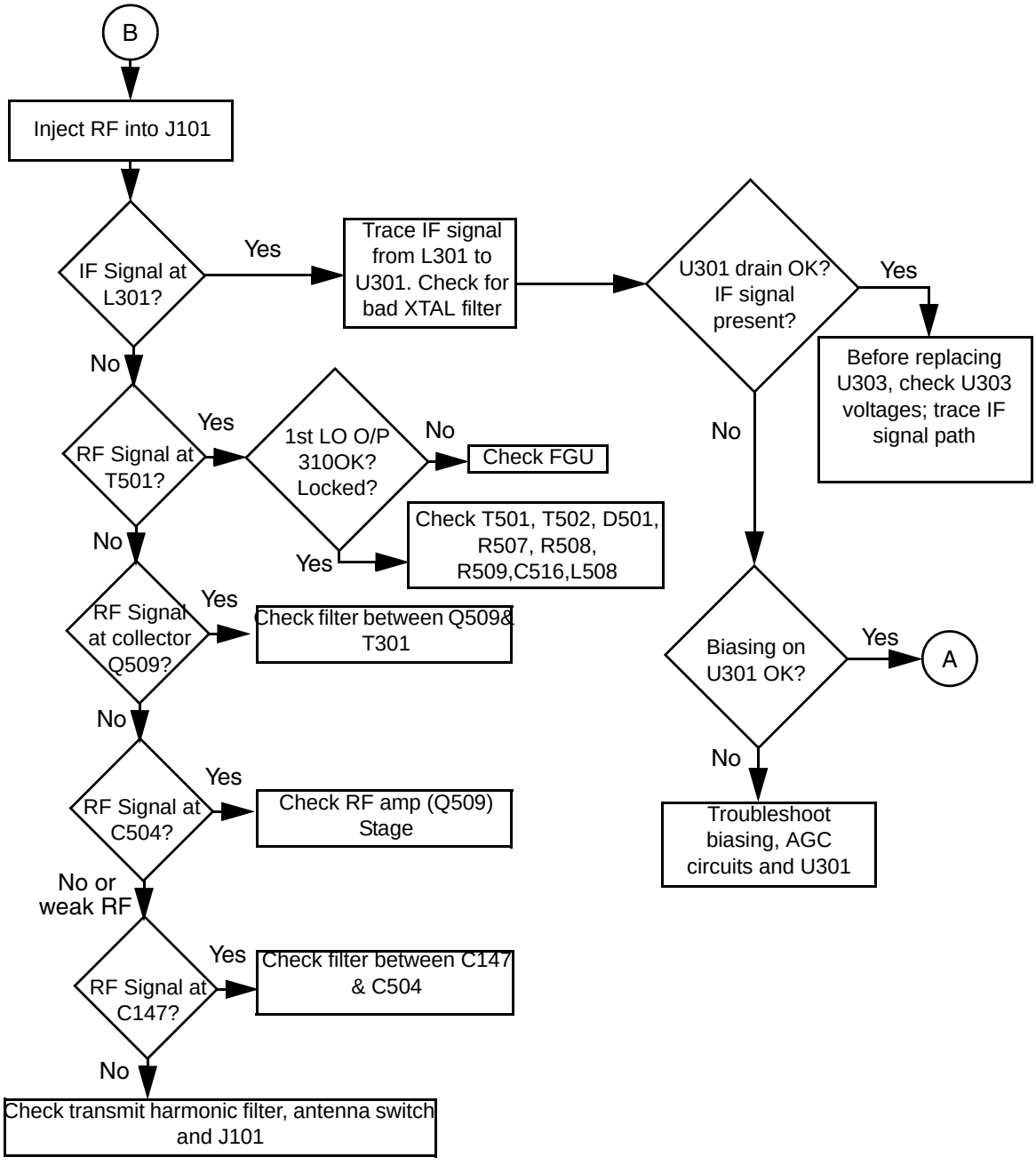
8.13.1 Troubleshooting Flow Chart for Controller



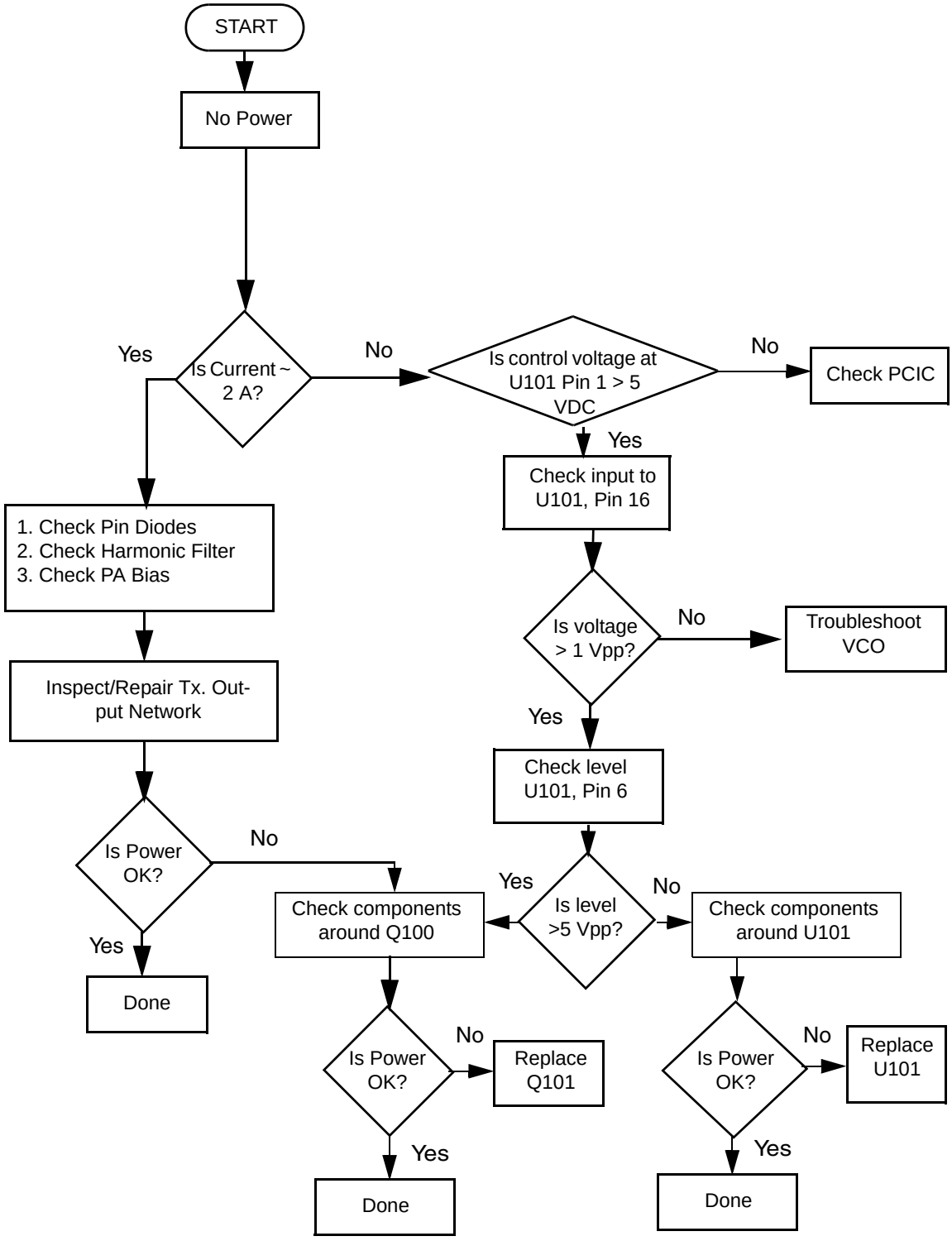
8.13.2 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



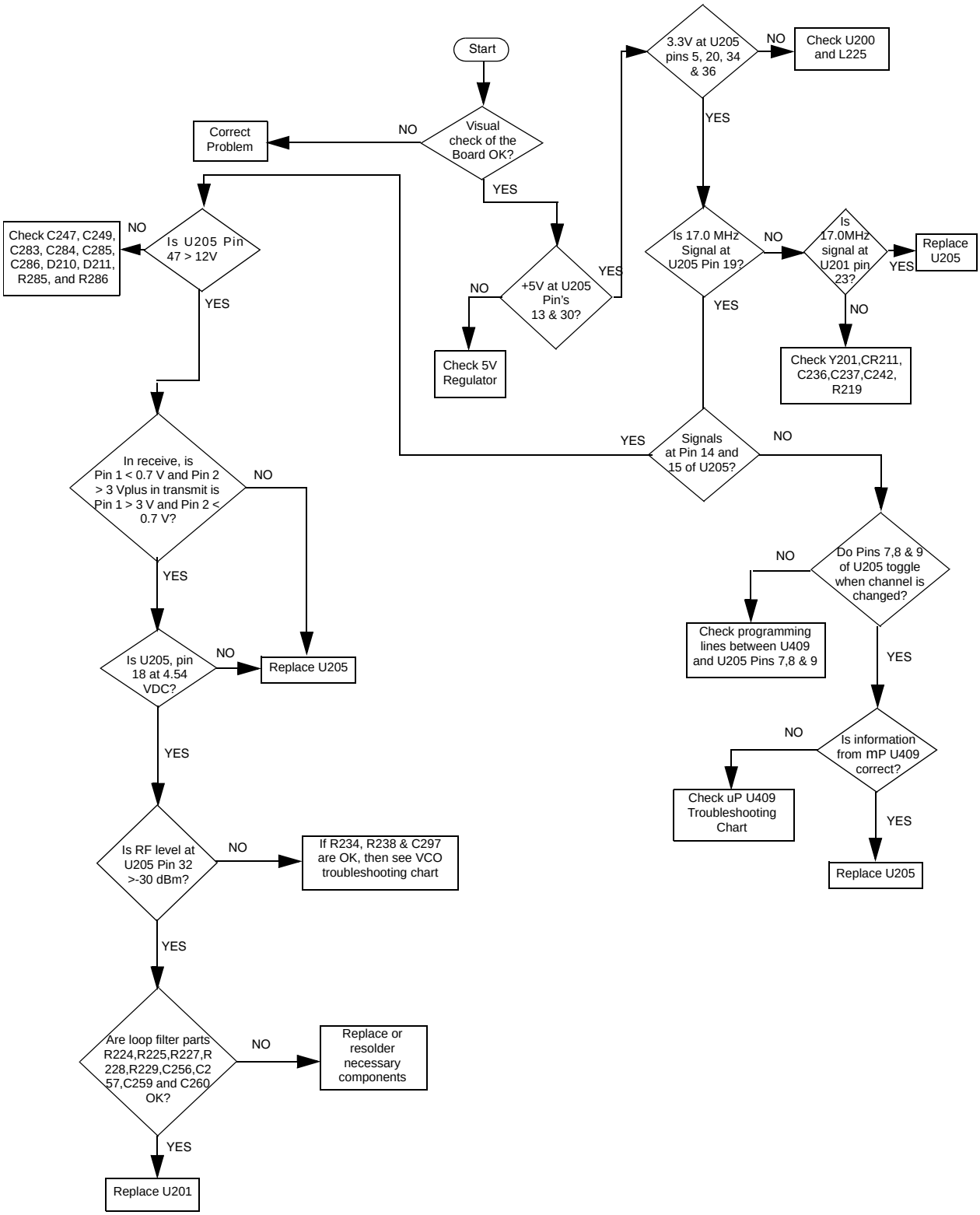
8.13.3 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



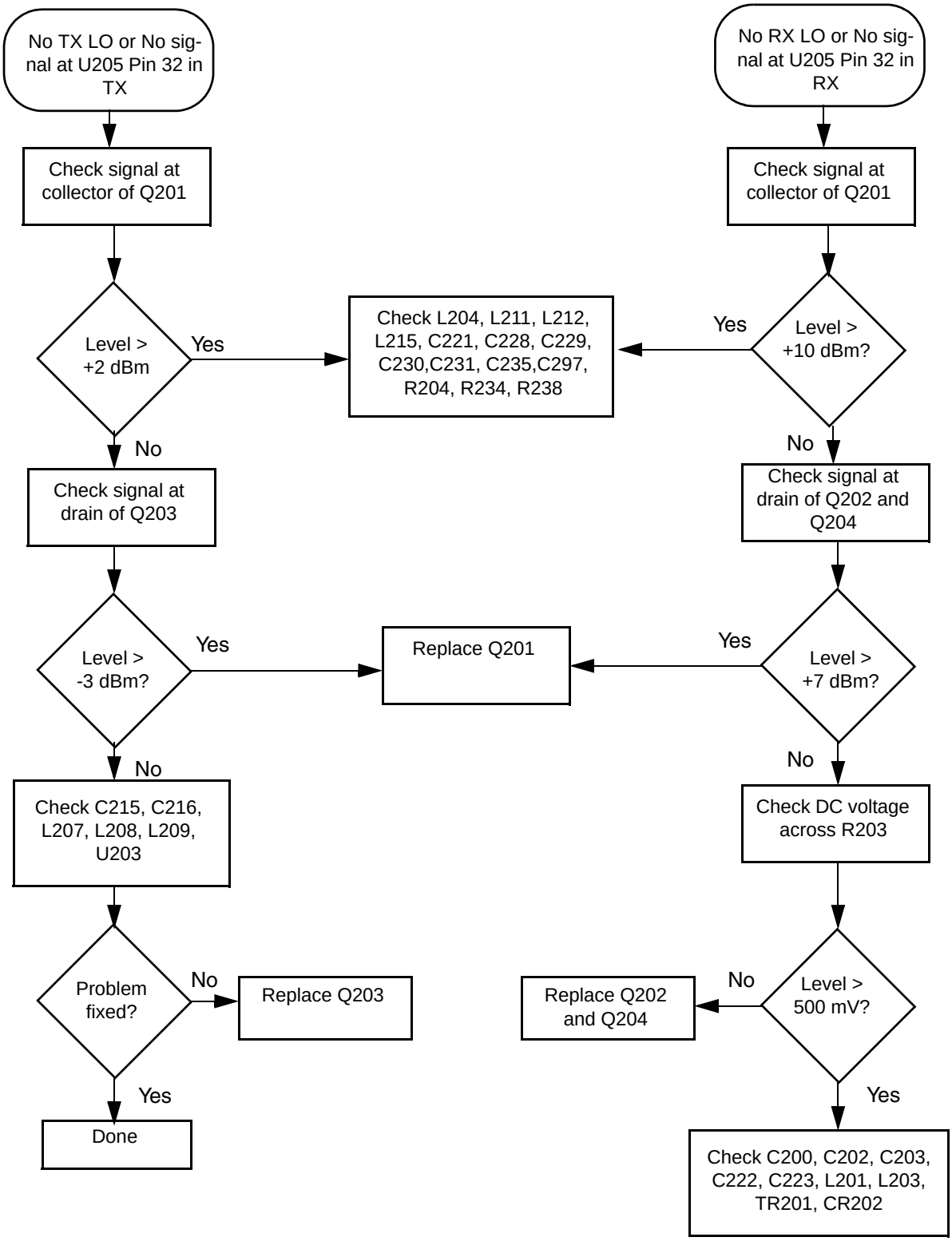
8.13.4 Troubleshooting Flow Chart for Transmitter



8.13.5 Troubleshooting Flow Chart for Synthesizer

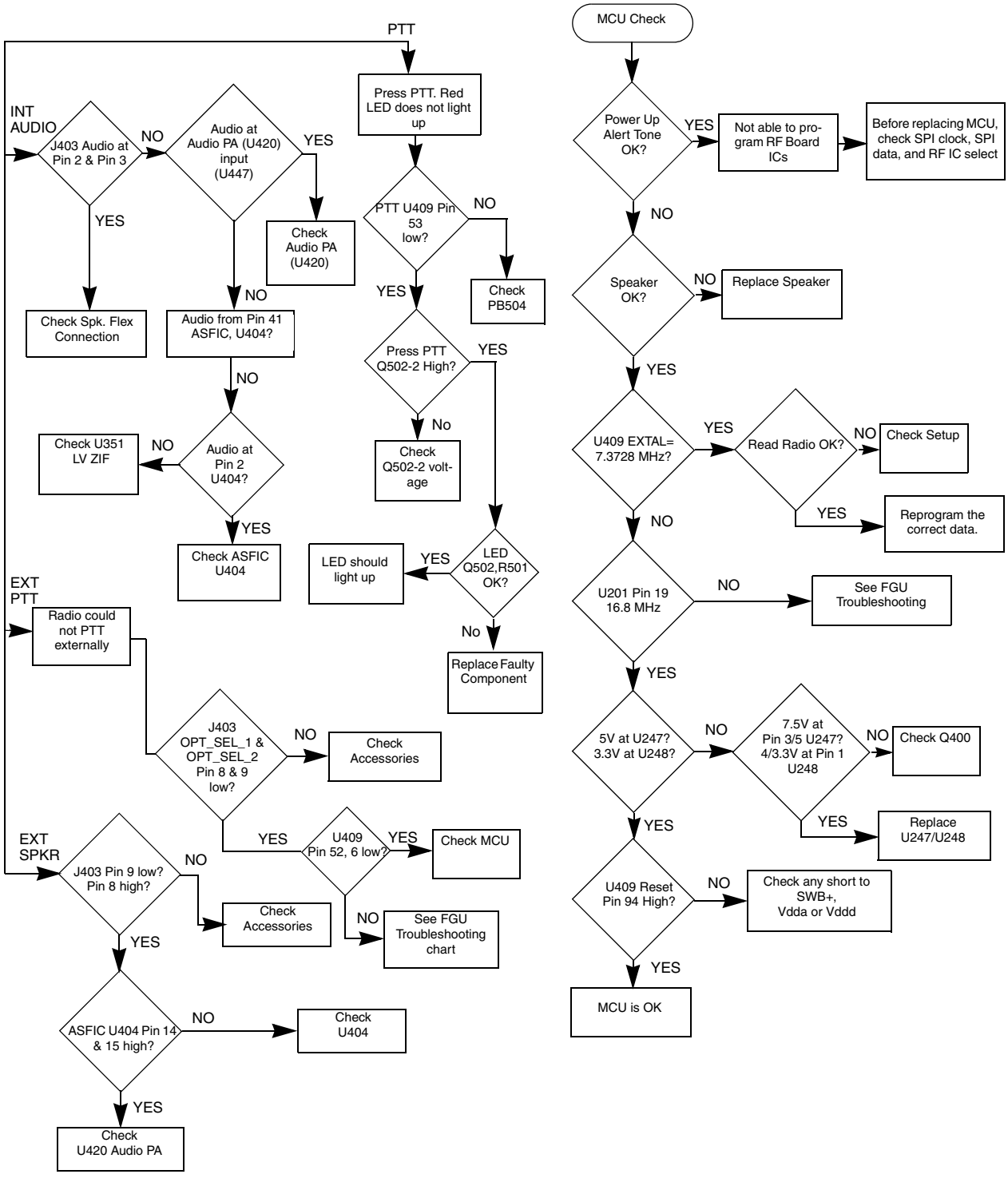


8.13.6 Troubleshooting Flow Chart for VCO

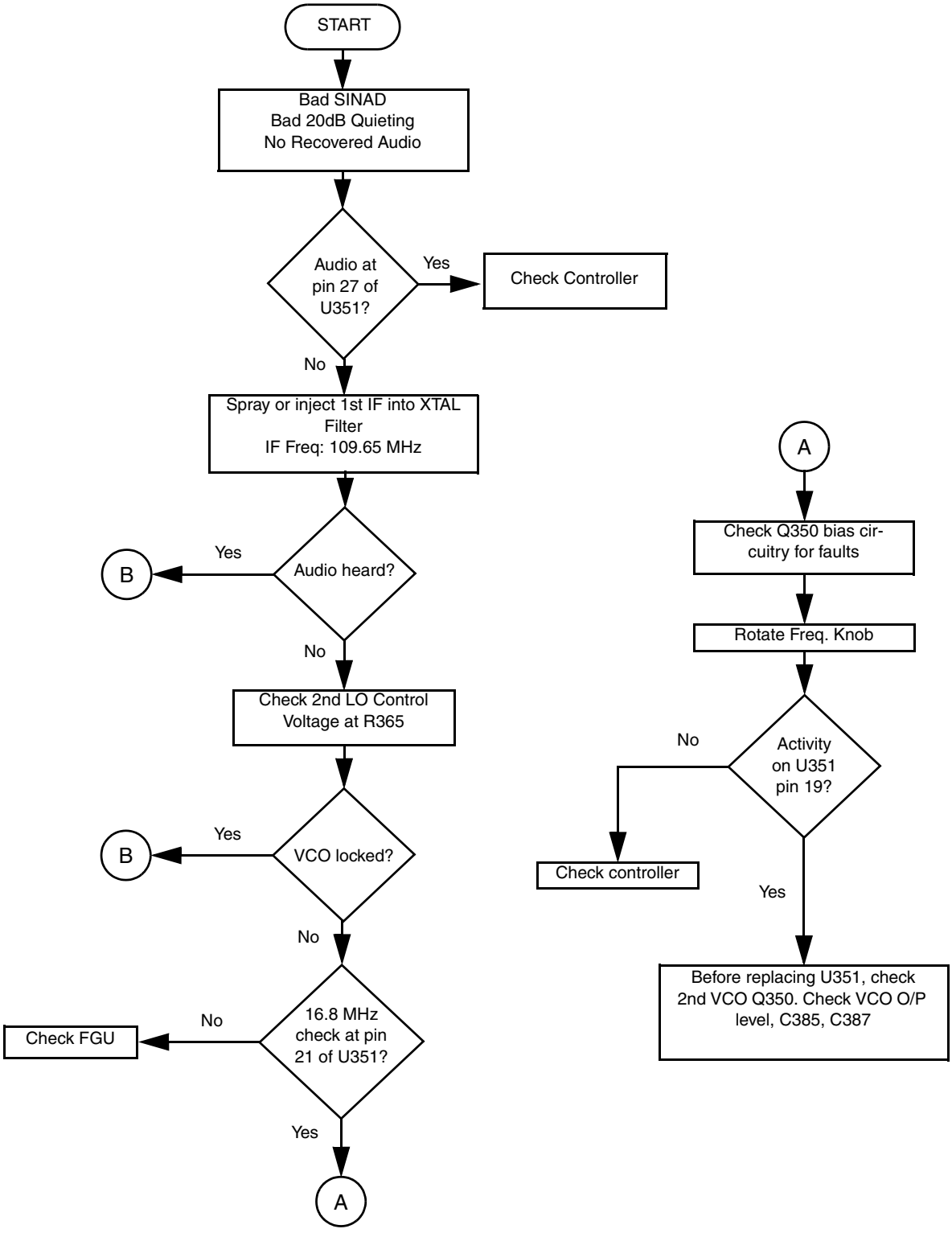


8.14 800 MHz Troubleshooting Charts

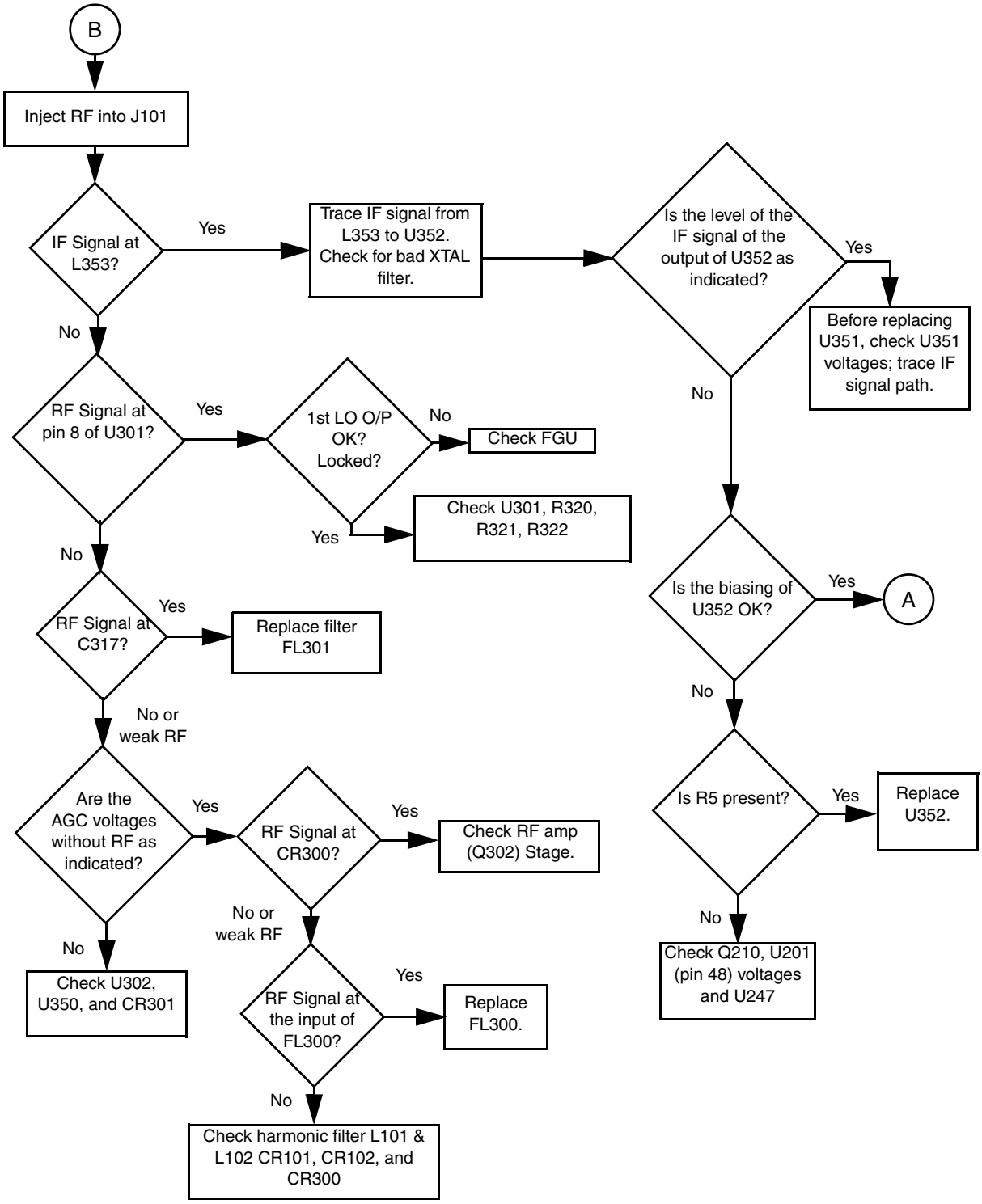
8.14.1 Troubleshooting Flow Chart for Controller



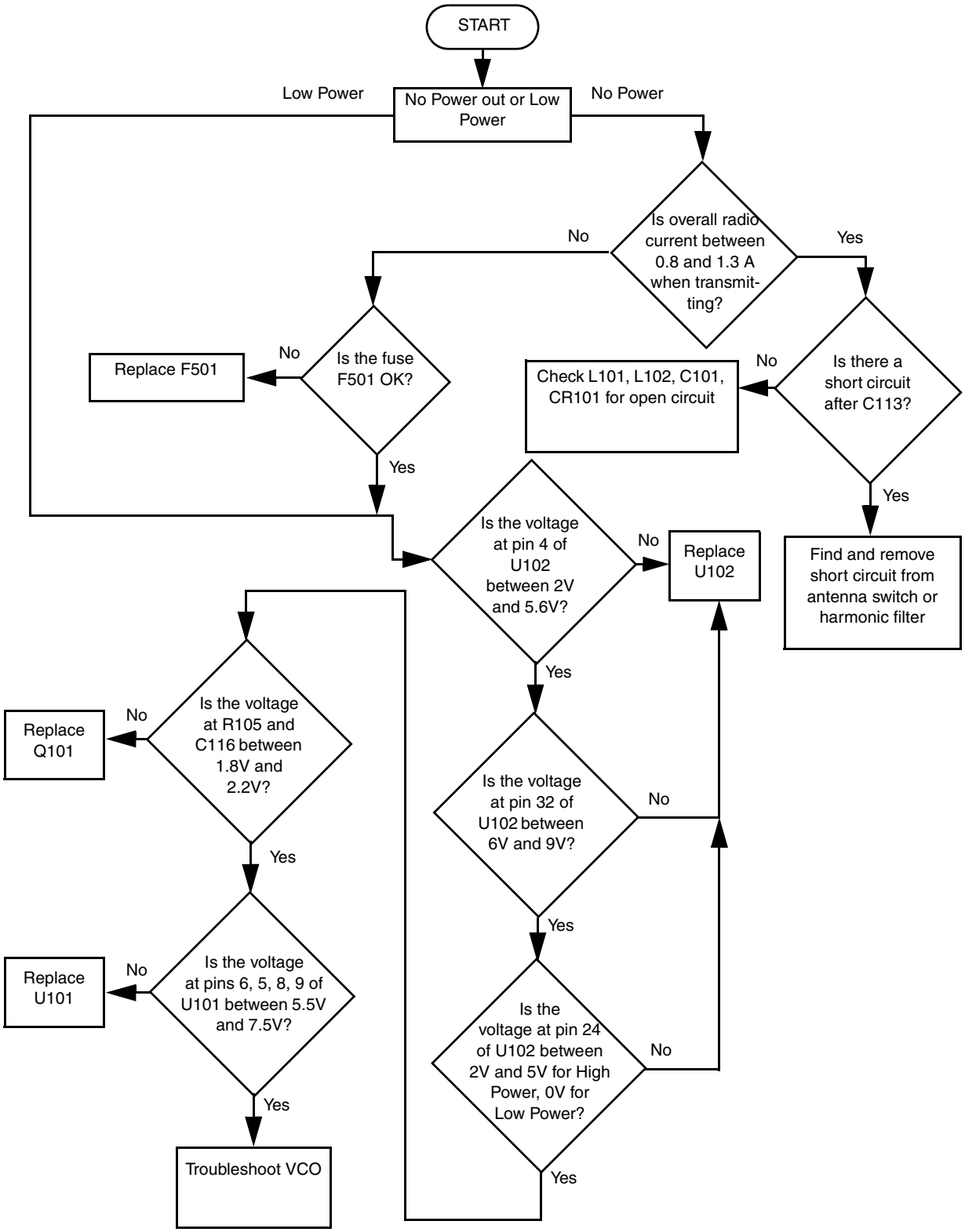
8.14.2 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



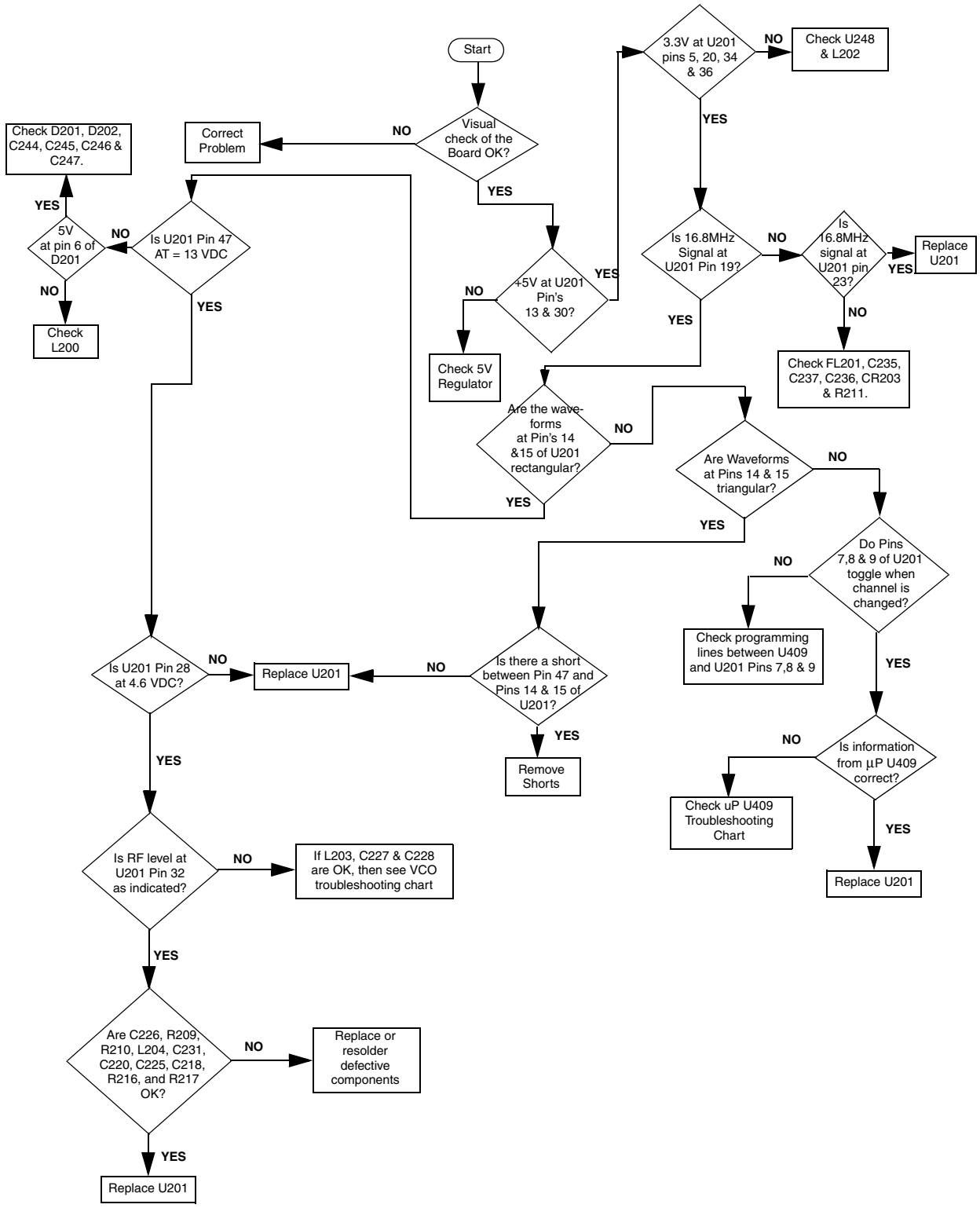
8.14.3 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



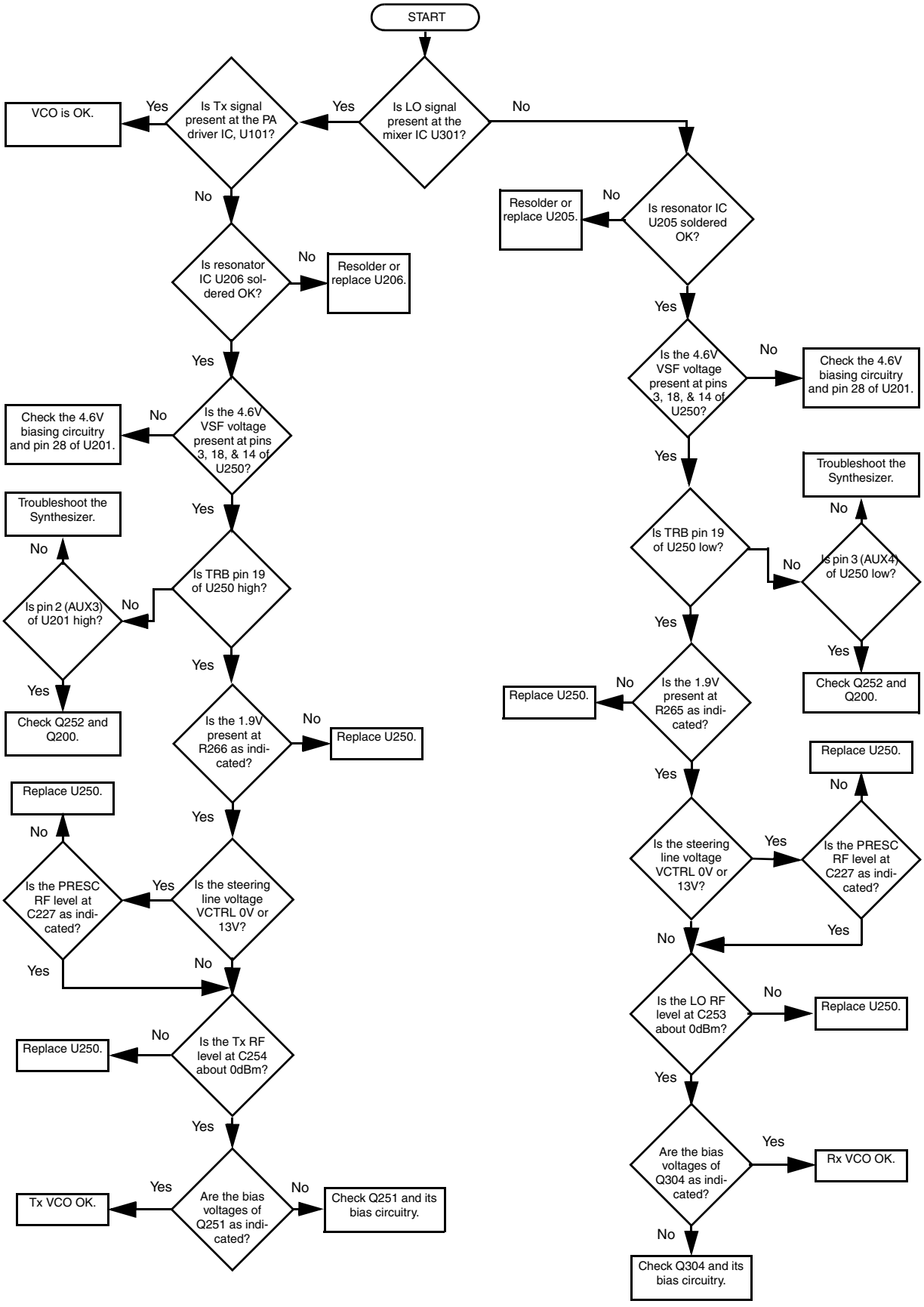
8.14.4 Troubleshooting Flow Chart for Transmitter



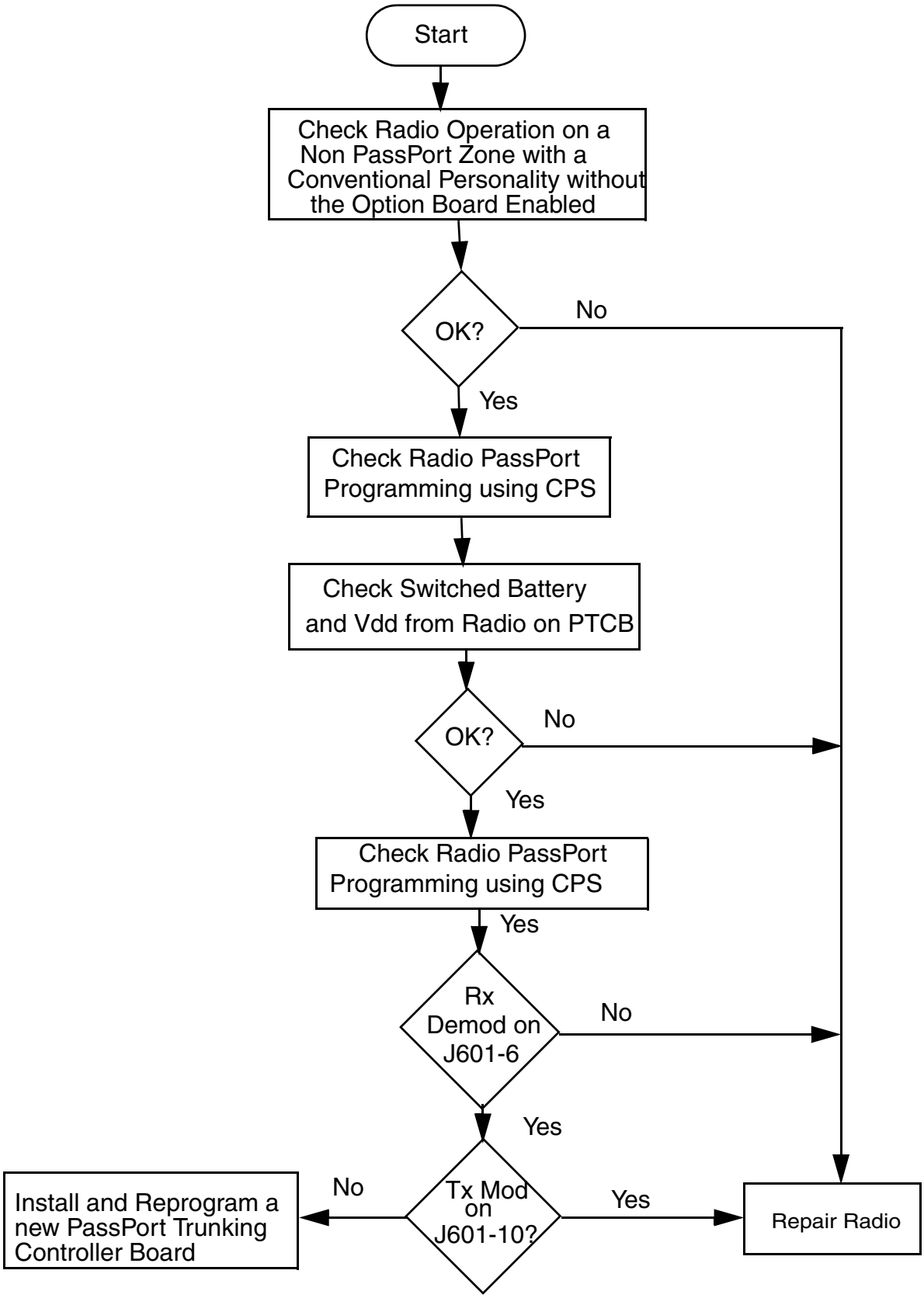
8.14.5 Troubleshooting Flow Chart for Synthesizer



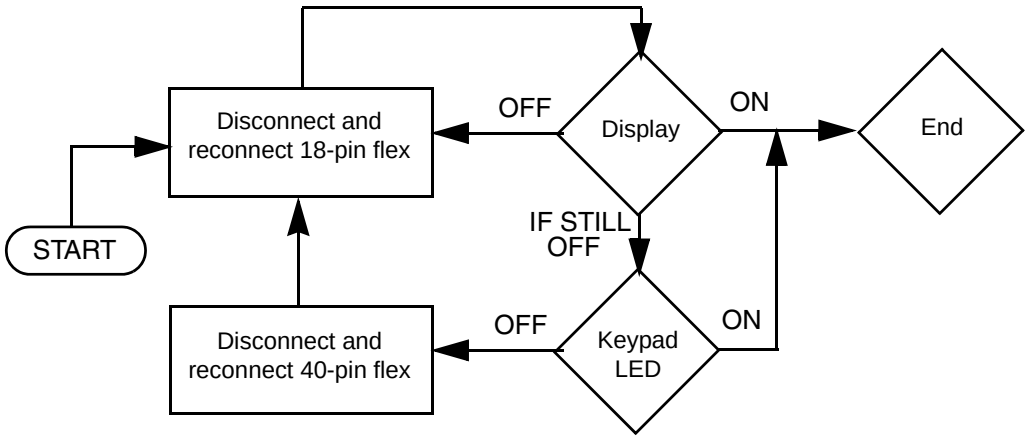
8.14.6 Troubleshooting Flow Chart for VCO



8.15 PassPort Trunking Troubleshooting Chart

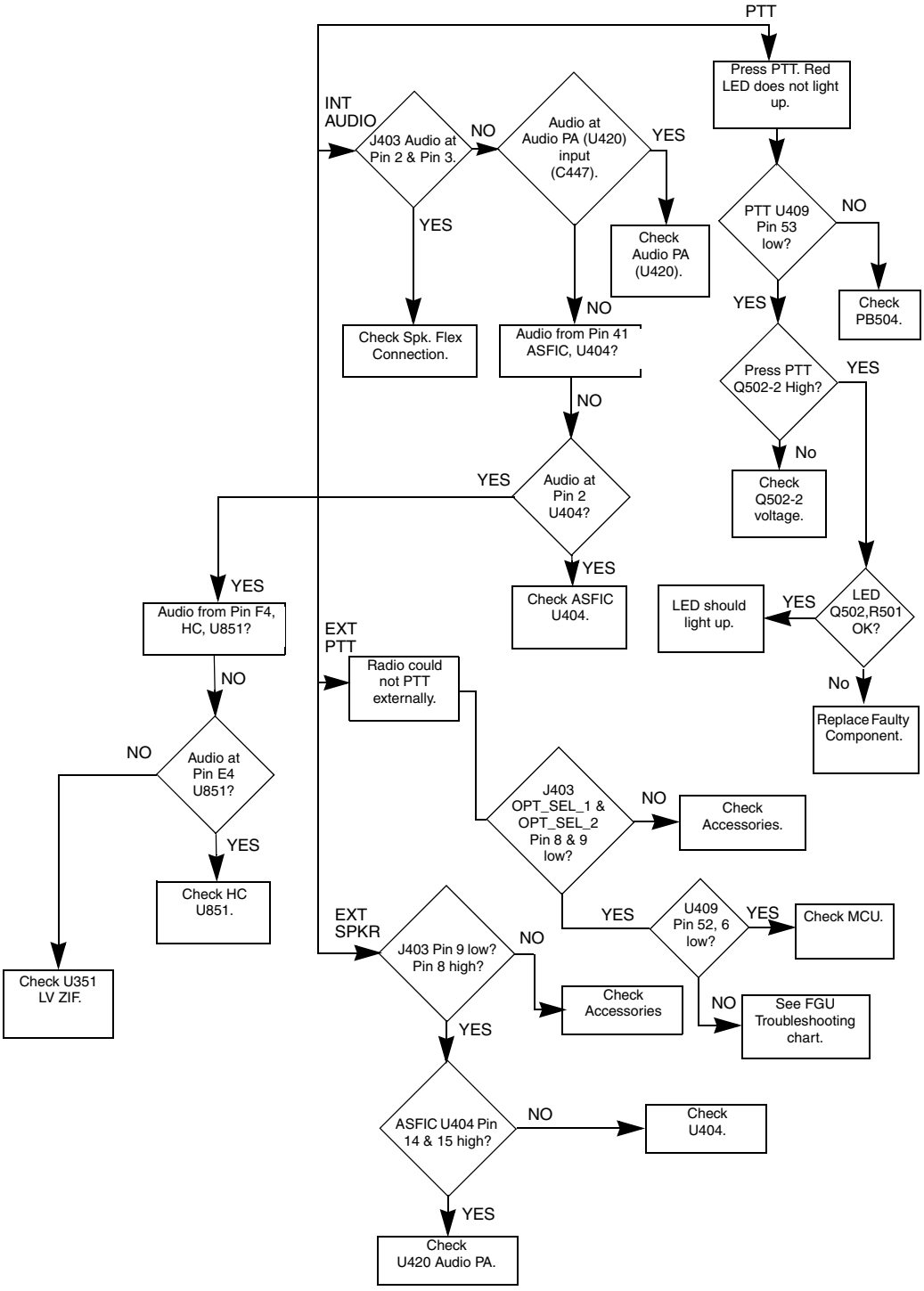


8.16 Keypad Troubleshooting Chart

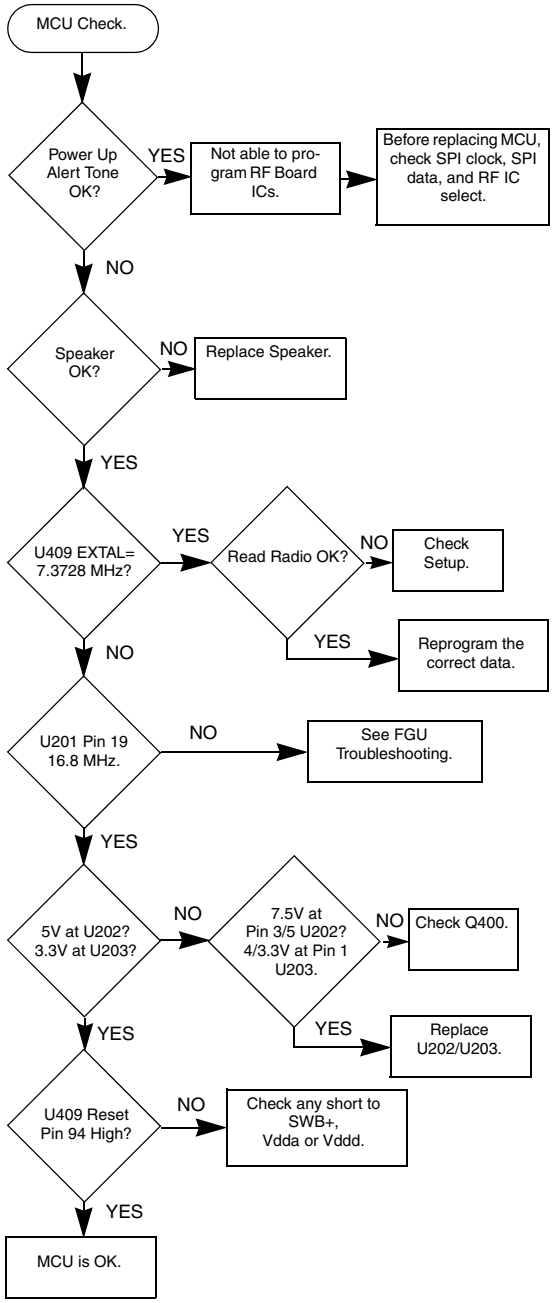


8.17 900 MHz Troubleshooting Charts

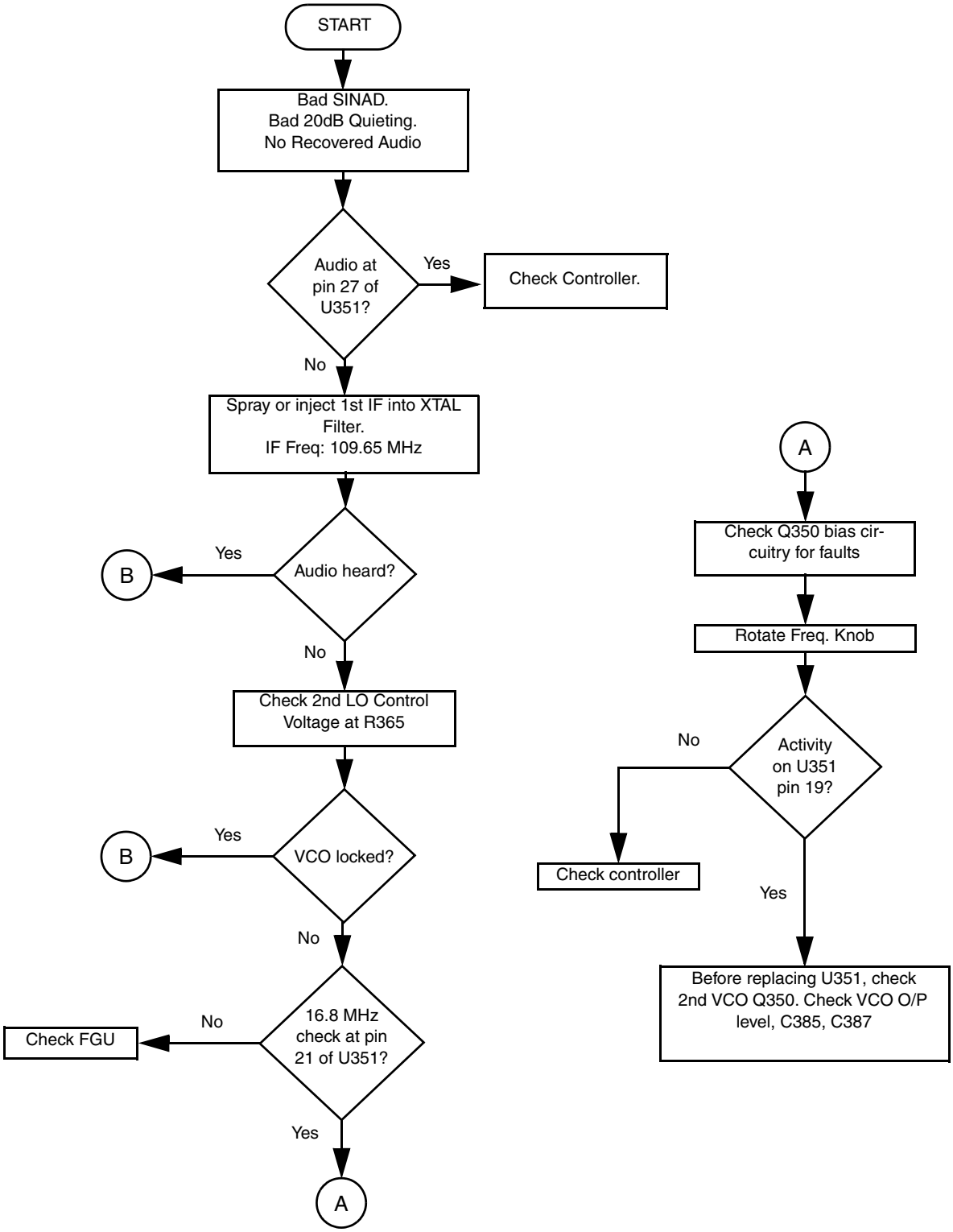
8.17.1 Troubleshooting Flow Chart for Controller (Sheet 1 of 2)



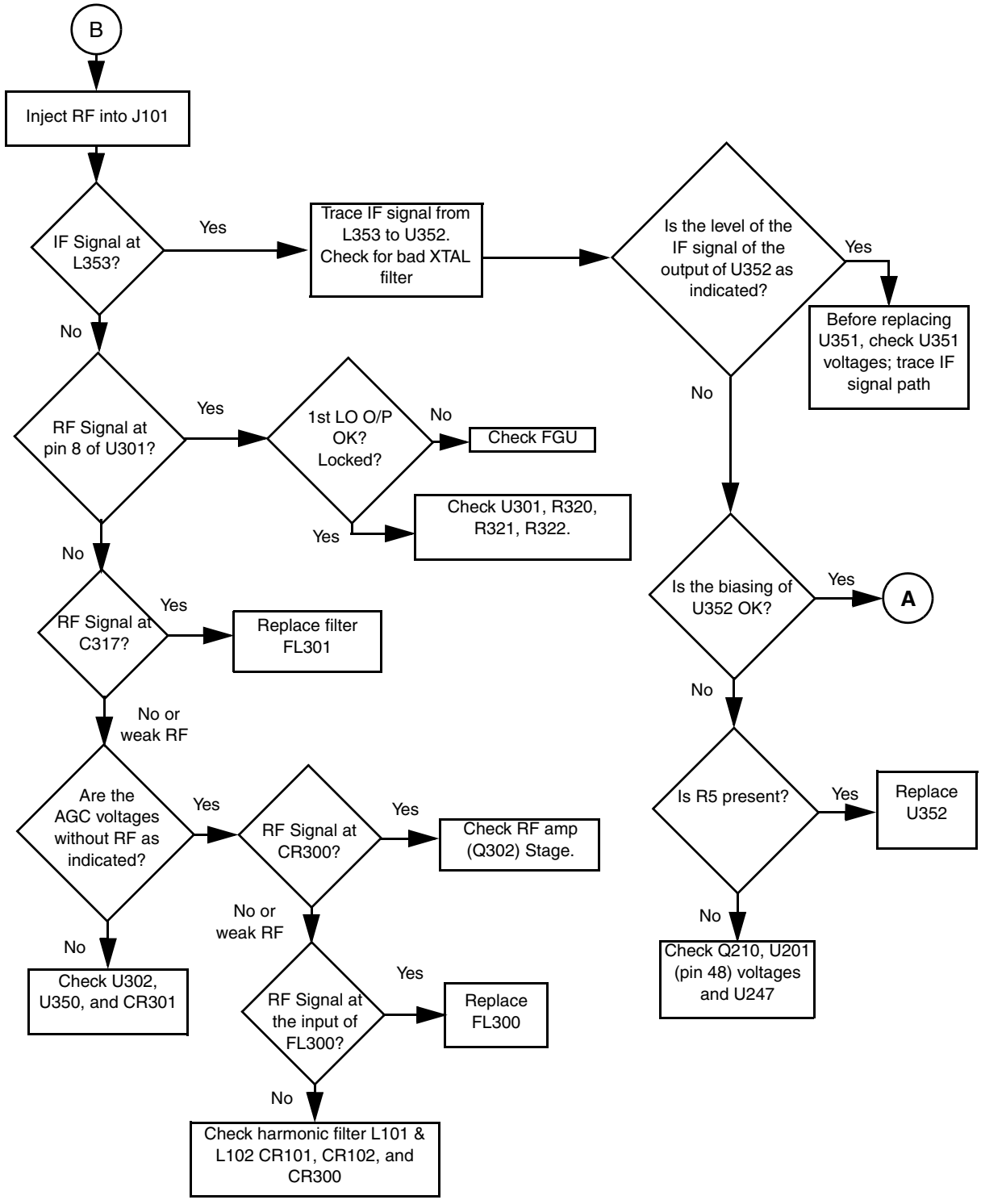
8.17.2 Troubleshooting Flow Chart for Controller (Sheet 2 of 2)



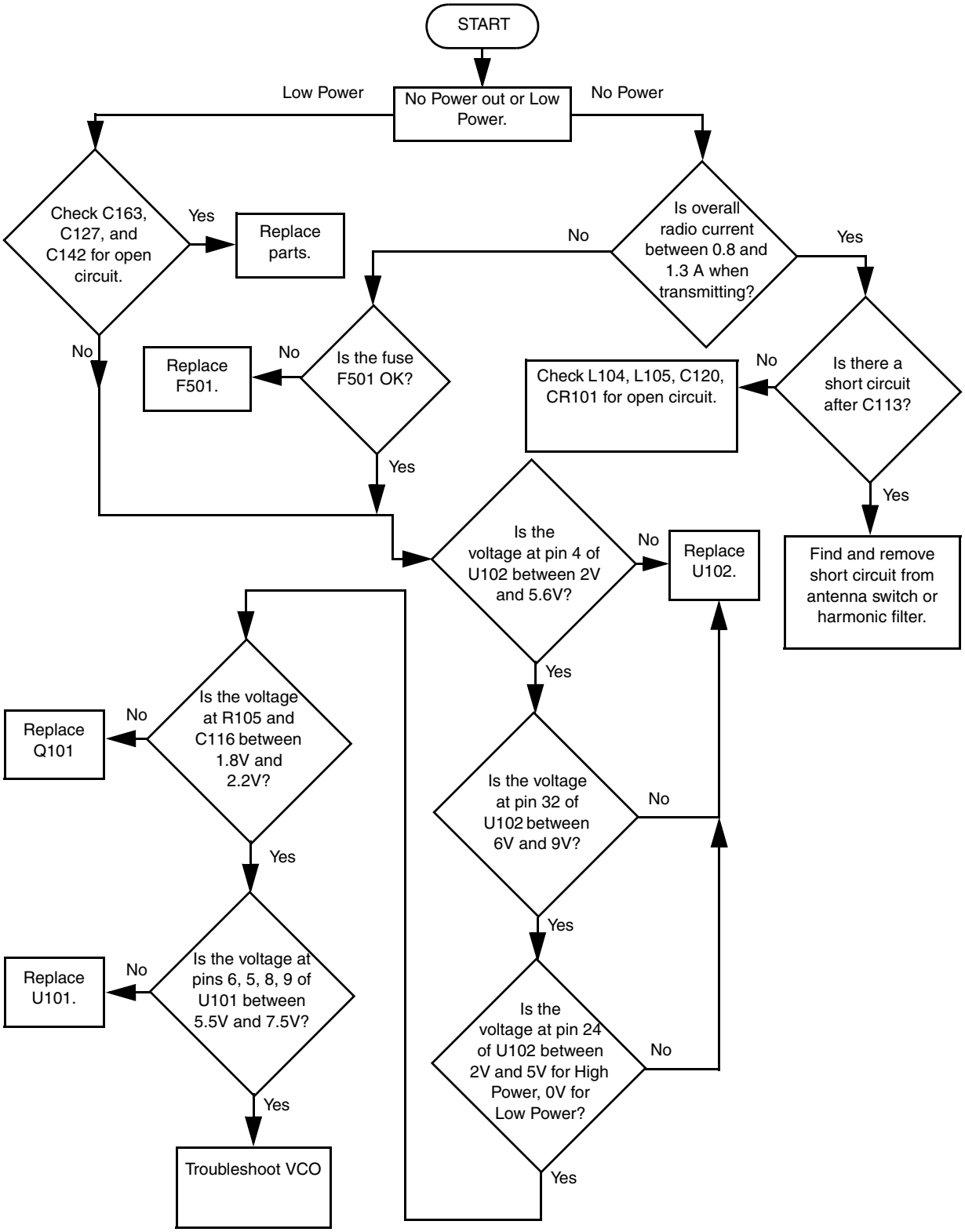
8.17.3 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



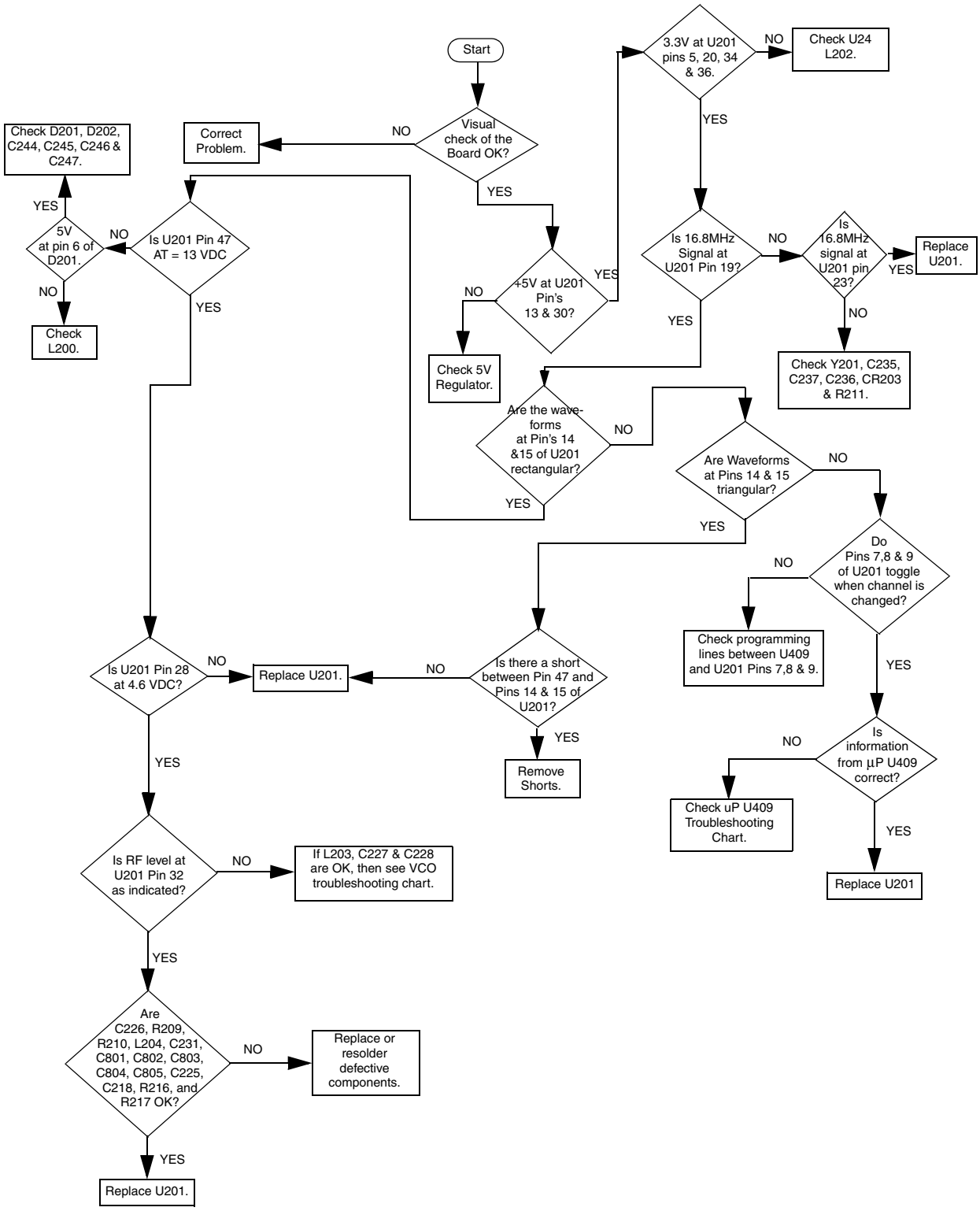
8.17.4 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



8.17.5 Troubleshooting Flow Chart for Transmitter



8.17.6 Troubleshooting Flow Chart for Synthesizer



8.17.7 Troubleshooting Flow Chart for VCO